NRC·CNRC

NRC Publications Archive
Archives des publications du CNRC

Simulation of the hole and current distributions in Si-Ge p-channel FETs with graded profiles

McAlister, S. P.; McKinnon, W. R.

This publication could be one of several versions: author's original, accepted manuscript or the publisher's version. / La version de cette publication peut être l'une des suivantes : la version prépublication de l'auteur, la version acceptée du manuscrit ou la version de l'éditeur.

Publisher's version / Version de l'éditeur:

Proceeding of the International Semiconductor Device Research Symposium (ISDRS'95), 2, pp. 599-602, 1995-12-08

NRC Publications Archive Record / Notice des Archives des publications du CNRC :
https://nrc-publications.canada.ca/eng/view/object/?id=a48607af-8b46-4e2e-ac6b-e3935e90f2e4
https://publications-cnrc.canada.ca/fra/voir/objet/?id=a48607af-8b46-4e2e-ac6b-e3935e90f2e4

Access and use of this website and the material on it are subject to the Terms and Conditions set forth at
https://nrc-publications.canada.ca/eng/copyright
READ THESE TERMS AND CONDITIONS CAREFULLY BEFORE USING THIS WEBSITE.

L'accès à ce site Web et l'utilisation de son contenu sont assujettis aux conditions présentées dans le site
https://publications-cnrc.canada.ca/fra/droits
LISEZ CES CONDITIONS ATTENTIVEMENT AVANT D'UTILISER CE SITE WEB.

Questions? Contact the NRC Publications Archive team at PublicationsArchive-ArchivesPublications@nrc-cnrc.gc.ca. If you wish to email the authors directly, please see the first page of the publication for their contact information.

Vous avez des questions? Nous pouvons vous aider. Pour communiquer directement avec un auteur, consultez la première page de la revue dans laquelle son article a été publié afin de trouver ses coordonnées. Si vous n'arrivez pas à les repérer, communiquez avec nous à PublicationsArchive-ArchivesPublications@nrc-cnrc.gc.ca.

National Research Council Canada | Conseil national de recherches Canada

Canada

Simulations of the hole and current distributions in Si-Ge p-channel FETs with graded Ge profiles

S.P. McAlister and W.R. McKinnon
Institute for Microstructural Sciences, National Research Council of Canada,
Ottawa K1A 0R6, Canada.

1. INTRODUCTION

Silicon-germanium channels incorporated into silicon field effect transistors give access to improved hole mobilities and add the capability of using bandgap engineering to improve the device performance. The use of Si-Ge in field effect devices has not been as well-studied as the use of Si-Ge in bipolar npn devices, where outstanding results have been achieved [1,2]. Both n- and p-channel FETs have been reported - the n-channel devices being grown on relaxed substrates and the p-channel devices have used strained layers. p-MOSFETs have been discussed and demonstrated by workers such as König and Schäffler [3], Verdonckt-Vandebroek et al. [4], and recently Voinigescu et al. [5], and references therein. An important consideration in the design of the devices is to optimize the Ge concentration and profile.

In this paper we show the simulations of the hole and current distributions in the different layers of a p-channel Si-Ge modulation-doped FET and examine how the bias and Ge profile in the Si-Ge alters this distribution. Since a gate oxide cannot be grown directly on a Si-Ge layer a thin layer of Si is needed between the Si-Ge channel and the gate. Inevitably some current flows though this parallel channel near the surface but the band offsets, all in the valence band in strained Si-Ge, help constrain the hole current. To adjust the threshold of the device a doped layer in the Si is needed. The dopant is most conveniently located in a layer beneath the Si-Ge channel. This then separates the holes from the acceptor dopants, which reduces the hole impurity scattering. Incorporating the dopants in the capping Si spacer would require an increase in its thickness and thus the channel-gate distance, leading to a reduction in the transconductance.

2. DEVICE STRUCTURE

We have simulated p-MOSFETs with a cross-sectional design (at the n+ polysilicon gate) as follows: 5 nm SiO_2, a 5 nm Si spacer, a 15 nm Si-Ge channel, 5 nm Si (all 3 layers are doped n-type at 1×10^{15} cm^{-3}), a 10 nm p-doped (1.5×10^{18} cm^{-3}) Si layer - all of which is on an n-doped (5×10^{16} cm^{-3}) Si substrate. In our simulations the devices are 1.5 μm long with 0.4 μm source and drain contacts and a 0.5 μm gate length. Source and drain contact dopings are Gaussian-shaped with maximum of 1.5×10^{18} cm^{-3} p-type. The choice of Ge profile is constrained by the total integrated Ge dose possible within the Matthews-Blakeslee limits. In this study we have restricted our discussion to 2 Ge profiles similar to that in other work [5]. The uniform channel design has a maximum Ge composition of 0.25, with a 0 to 0.25 Ge grading over 3 nm at the edges of the channel. The triangular profile has a Ge composition of 0.4 at 3 nm from the top of the channel - which is then graded down to 0 over the remaining 0.12 nm of the channel. The two profiles have the same integrated Ge dose. The Matthews-Blakeslee limit restricts the total Ge in a layer so we have chosen the Ge dose to keep the layers from undergoing strain relaxation. Note that we have used an n+ polysilicon gate and we do not discuss the p-polysilicon case which has been mentioned in [4].

In Fig. 1 the equilibrium band diagrams for the structures are shown to overlap except in the Si-Ge channel region. The incorporation of bandgap narrowing into the calculation makes the p-doped threshold-adjust region in the Si clearly evident. One major difference between the two profiles is the built-in field in the triangular profile design which moves the holes towards the gate.

3. Simulation Results

The simulations were performed using a commercial simulation package (*Atlas/Blaze*, Silvaco International), with a mesh of approximately 3000 nodes, and using Fermi-Dirac statistics and a drift-diffusion model. The interface oxide was chosen to be defect-free for this investigation. Hole mobilities were the same as in [5]. Most parameters have the usual Si values and expressions.

The current in the Si-Ge channel is not uniform under the gate especially near pinchoff. However when the channel is sufficiently long and the device is forward biased the center of the channel can be viewed as being representative of the effects of the different layers in the device. At the end of the channel, edge effects and those from the contacts become important and can obscure some of the main features we are attempting to illustrate. In the figures we used V_{DS} = -2.5V.

In Fig. 2 we show the integrated current under the center of the gate, and the contributions from the various layers, for the triangular and uniform Ge profile devices. In effect we write

$$I_{DS} = I_{Si\ cap} + I_{SiGe} + I_{Subs}\ .$$

The contribution from the substrate includes that from the doped threshold-adjust layer, which gives the majority of the contribution to the substrate current. It is only really important at low bias. In the range of gate voltage from -0.5 to -1.5V the Si-Ge channel dominates the response, which is can also be shown in a de-convolution of the transconductance. At higher biases the parallel current in the cap layer turns on and by -3V is greater than the contribution from the Si-Ge channel. This comment also applies to the transconductance. The effect of the cap turning on is to shield the Si-Ge channel from the gate. The triangular profile is better in confining the current to the Si-Ge channel in the -0.5 to -1.5V range. This becomes clearer if the distributions are viewed as a function of distance under the center of the gate. This is shown in Figs. 3 and 4 for the triangular and uniform profile designs, respectively. The data is also plotted on a logarithmic scale to highlight regions where the current is small. The distribution for the different biases depicted in these figures at first shows the increasing contribution to the current of the Si-Ge channel and how the parallel cap layer, which represents the normal Si FET current, eventually starts to dominate. The distribution of current in the Si-Ge layers reflects the Ge profile. In the triangular Ge profile case there is a built-in field that moves the holes away from the underlying acceptor dopants under the channel to the regions where the bandgap is smallest and the hole mobility optimum. Thus the asymmetric Ge profile achieves 2 desirable features at once. The current in the channel is sharply peaked similar to that at the oxide/Si interface at the highest biases. The logarithmic plot shows linear regions which reflect the linear variation of the potential with position - in the cap layer this is because the cap layer is similar to a capacitor, whereas in the channel it is because the separation of the valence band from the Fermi energy is dependent on the bandgap, which in turn is linearly dependent on position.

In the current distribution for the uniform Ge device (Fig. 4) the current through the Si-Ge channel is initially skewed towards the lower edge of the channel. This is due to the lack of a built-in field over the uniform Ge region. As a result the transconductance is not as good as for the triangular profile design. When the negative gate bias is increased the current distribution eventually becomes

skewed towards the top of the channel before the parallel current in the Si cap layer starts to increase. Eventually this latter current dominates. This is due to the transfer of the holes from the acceptors into the Si-Ge channel and then to the Si cap - which can be envisaged to occur when the band edges are moved up on the l.h.s. in Fig. 1 when the negative gate bias is increased. The uniform design spreads the current better across the Si-Ge than the triangular profile leading to smaller peak current densities in the channel, but at the expense of the slightly reduced performance. The double-peaked nature of the uniform profile's current distribution suggests a higher Ge concentration would be needed in the center of the channel to give a more uniform current distribution, however this would still be skewed at the extremes of the gate bias range.

The current distributions are partially representative of the hole distributions. In Fig. 5 we show the cross-sectional distribution on holes, corresponding to current distributions similar to those in Fig. 3. This cross-section is at the center of the gate. For clarity we show the region down to the p-doped threshold-adjust region - the dopant scale is logarithmic. To a first approximation the hole distribution looks like the current distribution. In Fig. 6 the hole distribution along the channel is shown for different gate biases for the uniform design at 2 positions in the Si-Ge profile. The distributions are at the 2 extremes of the uniform (0.25 Ge) region of the profile, i.e. at the positions where the current density is peaked. The cross-section at the top edge (solid curve) shows the hole density being reduced at the edge of the gate near the drain. For the cross-section for the lower position there are more holes near the edge of the gate near the drain than in the center of the gate. This shows that the current at the end of the Si-Ge channel tends to be distributed towards the lower part of the channel at the drain contact. We have seen similar effects in GaAs -based devices before [6].

The high frequency performance was also simulated and confirms the superiority of the triangular profile, with similar results as [5]. The current distributions we have shown suggest that the triangular profile could be further improved by raising the Ge concentration at the lower edge of the channel, at the expense of the layer thickness, ending up with a trapezoidal Ge profile. This design should spread the current better over the Si-Ge channel, make the current distribution closer to the gate at low bias and thus channel the hole current better in the Si-Ge layer to produce higher trans-conductance.

We thank Tracey Bradford for some initial simulations and Sorin Voinigescu for his help.

REFERENCES

[1] D.L. Harame, J.H. Comfort, J.D. Cressler, E.F. Crabbé, J.Y.-C. Sun, B.S. Meyerson and T. Tice, "Si/SiGe epitaxial-base transistors - Part 1: materials, physics, and circuits," IEEE Trans. Electron Devices, vol. 42, pp. 455-468, 1995.

[2] D.L. Harame, J.H. Comfort, J.D. Cressler, E.F. Crabbé, J.Y.-C. Sun, B.S. Meyerson and T. Tice, "Si/SiGe epitaxial-base transistors - Part 2: Process integration and analog applications," IEEE Trans. Electron Devices, vol. 42, pp. 469-482, 1995.

[3] U. König and F. Schäffler, "p-Type SiGe channel modulation doped field-effect transistors with post-evaporation patterned submicrometre Schottky gates," Electron. Lett., vol. 29, pp. 486-488, 1993.

[4] S. Verdonckt-Vandebroek, E.F. Crabbé, B.S. Meyerson, D.L. Harame, P.J. Restle, J.M.C. Stork and J.B. Johnson, "SiGe-channel heterojunction p-MOSFETs," IEEE Trans. Electron Devices, vol. 41, pp. 90-101, 1994.

[5] S.P. Voinigescu, P.B. Rabkin, C.A.T. Salama and P.A. Blakey, "2D numerical investigation of the impact of compositional grading on the performance of submicrometer Si-SiGe MOSFETs," IEEE Trans. Electron Devices, vol. 42, pp. 1039-1046, 1995.

[6] Z.-M. Li, S.P. McAlister and C.M. Hurd, "Use of Fermi statistics in two-dimensional numerical simulation of heterojunction devices," Semicond. Sci. Technol., vol. 5, pp. 408-413, 1990.

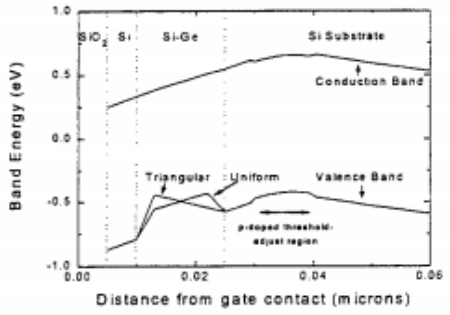

Fig. 1. Band diagram for the devices.

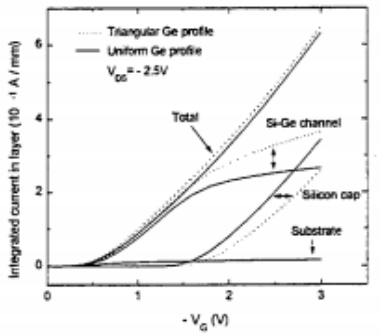

Fig. 2. Gate voltage dependence of the drain current and the contributions of the various layers to the drain current.

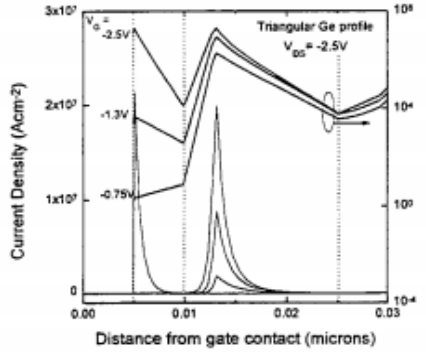

Fig. 3. Cross section of the current distribution, for the device with the triangular Ge profile, at the mid-point of the gate, at the indicated biases. Top curves use log scale on r.h.s.

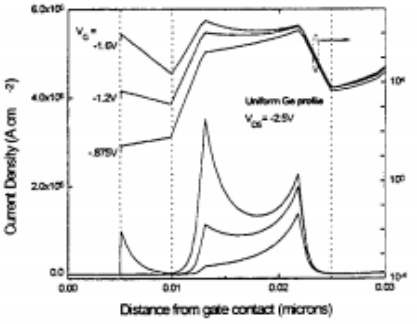

Fig. 4. Cross section of the current distribution, for the device with the uniform Ge profile, at the mid-point of the gate, at the indicated biases. Top curves use log scale on r.h.s.

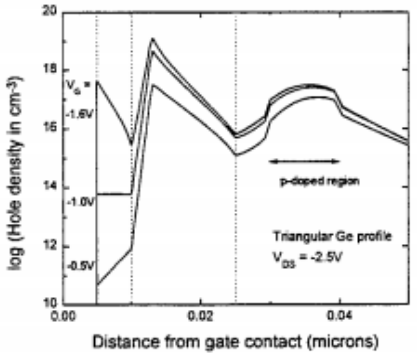

Fig. 5. Cross section of the hole distribution for the device with the triangular Ge profile, at the mid-point of the gate, at the biases indicated.

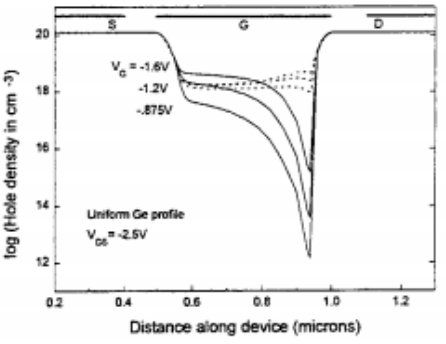

Fig. 6. Hole distribution along the channel for the uniform Ge profile device. Dotted curves are for the bottom edge of the graded region and solid ones for the top edge.