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Comprehensive Study on High Purity Semiconducting Carbon Nanotube Extraction

Tathagata Srimani, Jianfu Ding, Andrew Yu, Pritpal Kanhaiya, Christian Lau, Rebecca Ho, Jefford Humes, Christopher T. Kingston, Patrick R.L. Malenfant, and Max M. Shulaker*

Carbon nanotubes (CNTs) are a rapidly maturing emerging technology for next-generation energy-efficient digital Very-Large-Scale-Integrated (VLSI) systems. However, a major remaining challenge facing CNT field-effect transistors (CNFETs) are metallic CNTs, causing incorrect logic functionality and increased leakage power. As no CNT synthesis technique demonstrates a reliable path toward manufacturing 99.99% semiconducting CNTs (s-CNT; required purity for VLSI systems), significant work focuses on solution-based sorting of CNTs (selectively removing metallic CNTs post-synthesis). Yet, there lacks both well-controlled comparisons carefully optimizing key processing parameters simultaneously (CNT synthesis sources, polymer additive used for selective sorting, etc.), as well as statistically significant electrical transistor characterization sample sizes to form concrete conclusions. Here, >90 000 CNFETs (totaling >90 million CNTs) are fabricated and characterized to demonstrate the following key advances: 1) systematic exploration of the impact of different combinations of CNT synthesis sources and polymer additives on the electrical performance of transistors (analyzing on-current, off-current, on off ratio, and threshold voltage) to find the best combination, 2) how the optimization and choice of the CNT source can be decoupled from that of the polymer, and 3) an optimal CNT solution that achieves >99.99% s-CNT purity using electrical measurements, meeting the requirement for VLSI systems.

1. Introduction

Physical and equivalent scaling of silicon-based field-effect transistors (FETs) has been a major driving force improving computing energy efficiency for decades. However, continued silicon scaling is growing increasingly challenging,[1–3] motivating research on emerging nanotechnologies as a potential future supplement to silicon-based systems.[4–12] For instance, one-dimensional carbon nanotubes (CNTs) are cylindrical nanostructures comprised of a single atomic layer of carbon atoms and have exceptional electrical, mechanical and thermal properties.[1–3] Carbon nanotubes can be used to form carbon nanotube FETs (CNFETs), which are a leading candidate for realizing energy-efficient digital circuits.[4–13] CNFETs (illustrated in **Figure 1**) follow the same general structure as traditional silicon metal-oxide-semiconductor FETs (MOSFETs) with lithographically defined source, drain and gate regions, but with CNTs forming the channel of the transistor instead of silicon.[14–19] Owing to CNT's ultrathin body as well as superior carrier transport,[14,16] digital VLSI circuits made from CNFETs are projected to achieve >7× energy efficiency benefit (characterized by energy-delay product, or, EDP) over similar systems made using silicon FETs even when compared at futuristic highly scaled 2 nm technology node.[19–20,21] There has been rapid progress in developing high performance CNFETs and CNFET-based CMOS digital circuits, progressing from a single-bit Turing-complete computer to a complete 16-bit RISC-V microprocessor.[1,16–17,22–33]

Yet despite this progress, experimental measurements of CNFETs often exhibit substantial off-state leakage current (I_{OFF}) due to presence of metallic CNTs. At the circuit level, this results in substantially increased leakage power and potentially even incorrect logic functionality.[1,34–36] To address this major challenge at the design level, Hills *et al.*[1] developed a circuit design technique known as *Designing REsliency Against Metallic CNTs* (*DREAM*), which reduces the s-CNT purity requirement of a digital VLSI circuit from 99.999999% to 99.99%, without imposing any additional processing steps. To meet this requirement, a wide variety of techniques have been investigated. For

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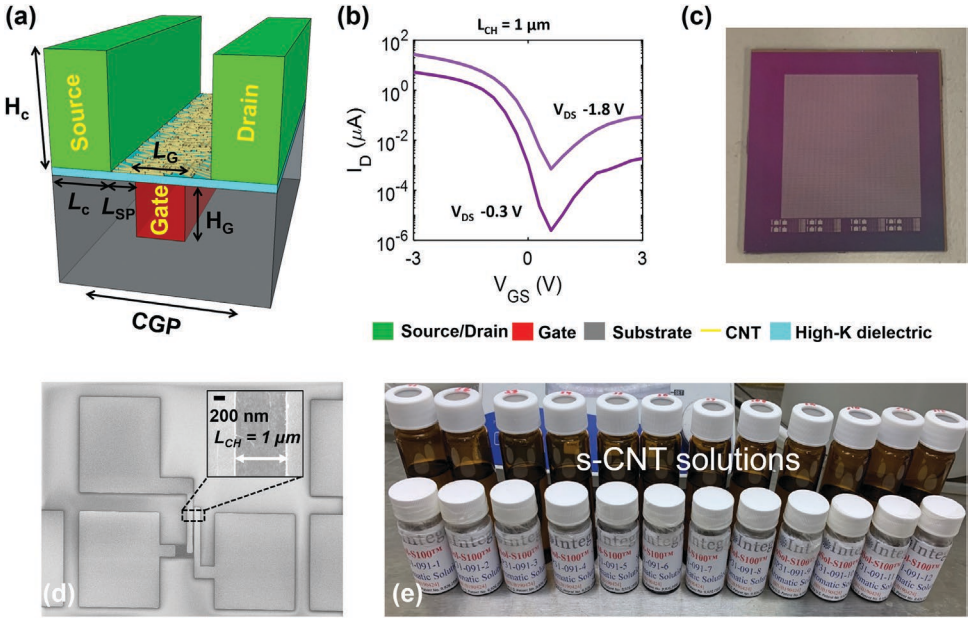

Figure 1. a) Schematic of back-gate CNFET. L_{CH} is the physical channel length, L_{SP} is length of the intrinsic CNT region. b) Experimentally measured I_D-V_{GS} characteristics for a transistor with L_{CH} = 1 µm (measured at room temperature). Device parameters listed in Table 2. c) Die Micrograph d) Scanning Electron Microscopy (SEM) images of fabricated CNFETs (channel zoomed in top right). e) s-CNT solutions tested for understanding the impact of precursors (CNT source, polymers, etc).

instance, multiple works have attempted to modify CNT synthesis conditions to primarily synthesize s-CNTs. While successful, the highest purity reported is only ≈99% s-CNT purity (measured optically) on only small-area substrates.[37–38] Thus, significant work has attempted to remove remaining m-CNTs postsynthesis, primarily through solution-based sorting[46] (ranging from gradient-density centrifugation to DNA assisted chromatographic purification to aqueous two-phase separation to conjugated polymer extraction). Yet despite years of progress, no single approach has been shown to meet all requirements, as it either does not achieve sufficient s-CNT purity (The best reliable solution sorting techniques report a s-CNT purity estimate of around 99.9% optically.[39] Approaches that involve electrical testing of CNFETs to characterize the s-CNT purity,[17,42–43] either use measurements at low drain bias (V_{DS}) which improves the I_{ON}/I_{OFF} ratios,[16,44] or do not use a large enough sample size of transistors to measure purtiy accurately. These techniques although correct in theory lead to very optimistic estimates of solution-based s-CNT purity.), or, introduces contaminants which prohibit use within commercial semiconductor manufacturing facilities, or, is difficult to scale to high-volume production. What hinders progress is that each approach has multiple parameters that can be tuned independently, creating a massive design space of permutations which is challenging to explore. For instance, consider conjugated polymer extraction,[37] the *only* commercially available approach that has been integrated within commercial silicon foundries and major semiconductor manufacturing facilities so far.[40–41] With this technique, different CNT synthesis sources can be initially chosen to generate the raw starting materials. And then different conjugated polymers can be chosen to selectively sort for the s-CNTs.

In this work, we demonstrate for the first time that conjugated polymer extraction can achieve the required >99.99% s-CNT purity for VLSI systems – confirmed through extensive electrical measurements and characterization. This is accomplished by systematically synthesizing, fabricating, and characterizing permutations of CNT synthesis sources and conjugated polymer choices, resulting in the optimal CNT solution. Moreover, through this detailed analysis, we also demonstrate that the ideal CNT synthesis source as well as the ideal conjugated polymer used for sorting are independent from one-another. This important observation enables both to be optimized independently, greatly simplifying future CNT solution optimization work.

1) PFDD: poly(9 9-di-n-dodecylfluorene-2 7-diyl)
2) PFPy: poly[(9,9-di-n-dodecylfluorenyl-2,7-diyl)-alt-(2,6-pyridine)].
3) PFBPy: poly[(9,9-di-n-dodecylfluorenyl-2,7-diyl)-alt-(5,5'-(2,2'-bipyridine)].
4) PCz: poly[9-(1-octylnonyl)-9H-carbazole-2,7-diyl].

2. Fabrication

The CNFET fabrication process has been reported previously and is described in ref. [1]. Figure 1a,b shows the schematics and measured electrical transfer characteristics (I_D-V_{GS}) of a typical back-gate p-channel CNFET. We use locally back-gated CNFETs for this study since they follow the fabrication process that is integrated in commercial foundries at a scaled ≤130 nm technology node and have been used to realize uniform and reproducible CNFETs and CNFET logic over 200 mm substrates.[40–41] s-CNTs dispersed in a solvent (described below) are deposited at room temperature directly onto pre-fabricated high-k dielectric/metal gate stack on silicon substrates (see "Experimental Section/Methods" for gate dielectric and contact metal). Scanning electron microscopy (SEM) images of typical CNFETs after

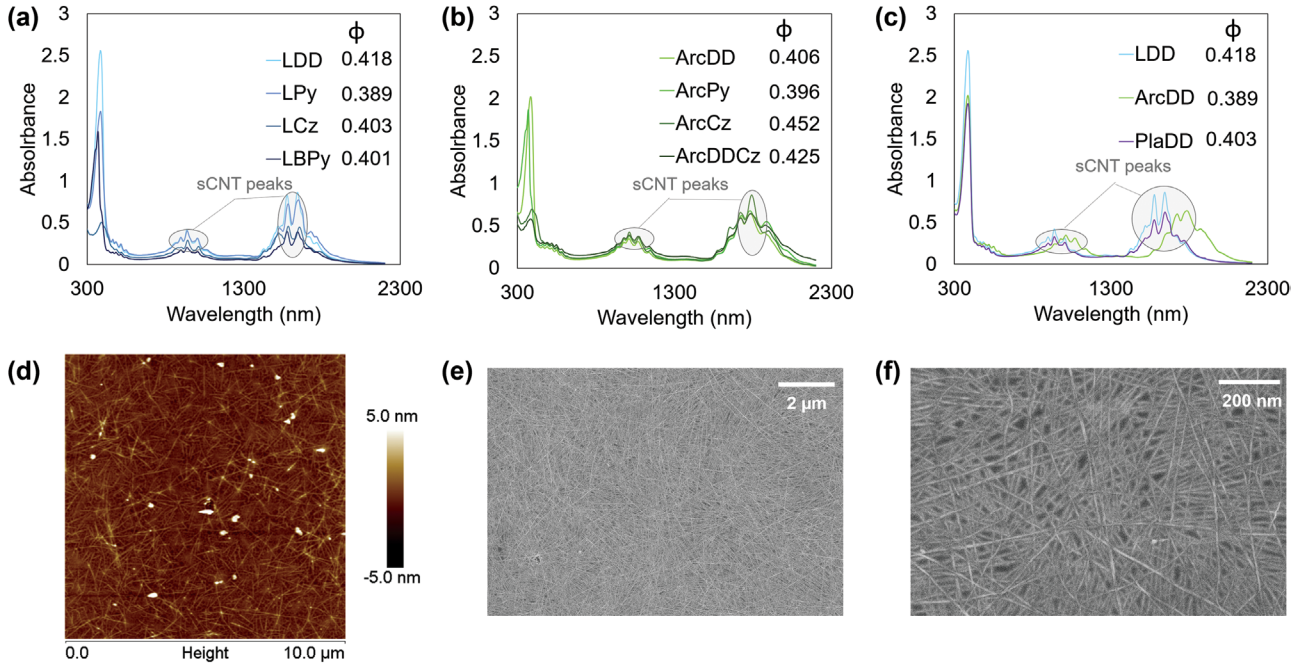

Figure 2. UV-Vis-NIR spectroscopy of s-CNT solutions (acronyms are listed in Table 1, color coded to match Figure 3, 4 and 5) a) for laser ablation CNTs wrapped with different polymers -PFDD, PFPy, PCz and PFBPy b) for arc discharge CNTs wrapped with different polymers – PFDD, PFPy, PCz and PFDD-Cz by polymer exchange c) for laser ablation, arc discharge and plasma CNT sources wrapped with the same polymer – PFDD. Measured absorption peak ratios (ϕ) from UV-Vis-NIR spectrum for each solution is reported in the legend as a qualitative optical estimate of the solution s-CNT enrichment (more details can be found in prior works[39]). Although higher ϕ may indicate higher s-CNT content, it cannot differentiate between low band-gap CNTs and metallic CNTs. d) AFM characterization of CNT length for laser ablation CNTs (LDD, same methodology is applied to estimate CNT length for each solution, illustrated in Figures S3–S5 in the Supporting Information). e,f) SEM characterization of uniform CNT deposition on top of die surface for laser ablation CNTs (LDD solution, SEMs for other solutions are shown in Figure S2 in the Supporting Information).

CNT deposition can be seen in **Figure 2**e,f. Following deposition of the CNTs, CNTs outside of the channel region of the CNFETs are removed by etching with oxygen plasma. Finally, source and drain contacts are aligned to the pre-fabricated gate stack and lithographically defined. A detailed process flow is shown in Experimental Section/Methods.

For the CNT solutions, as described previously, an extremely diverse combination of CNT synthesis sources and conjugated polymers have been investigated in the literature. Here, we restrict our analysis to the leading contenders based on literature.[45–46] For the starting CNT material, the CNT synthesis source is chosen to be either Arc Discharge, Laser Ablation, or Plasma. For the conjugated polymer, we use either PFPy, PFDD, PCz, or PFBPy (listed in **Table 1**, see further details in methods). As the preparation of the CNT solutions is a critical aspect of this work, we detail the full process flow below.

The enhanced hybrid conjugated polymer extraction (eh-CPE) process includes a traditional hybrid conjugated polymer extraction (h-CPE) and then a final conditioning treatment.[39] The eh-CPE process is started by dispersing a mixture of acid treated raw SWCNTs (obtained from different synthesis sources) with the polymer PFDD (or PCz) in toluene at ≈1/1 of polymer to CNT (P/CNT) ratio in all the different starting solutions. Each solution went through a sonication step (30-minute tip sonication) followed by an ultracentrifugation step (30 minutes, 12500 rpm, RCF: 23700 g). The extracted solution (i.e., the supernatant) was mixed with silica gel, sonicated (30 minutes), and then centrifuged (30 minutes, 12500 rpm). The supernatant collected from this centrifugation step was filtered using a PTFE membrane to collect a black film of PFDD (or PCz) wrapped CNTs with a polymer/CNT ratio of ≈1/1. For the samples with a polymer other than PFDD or PCz (i.e., PFPy and PFBPy), a polymer exchange step was performed on the black film of PFDD wrapped CNT, to completely replace PFDD with the corresponding polymer (i.e., PFPy and PFBPy). The polymer exchange[47] step was performed as follows. First, PFPy

Table 1. Solution Properties.

Sample	CNT source	Polymer	Solution $\Phi^{a)}$	P/CNT
LDD	Laser Ablation	PFDD	0.418	4.04
LPy	Laser Ablation	PFPy	0.389	5.42
LCz	Laser Ablation	PCz	0.403	8.15
LBPy	Laser Ablation	PFBPy	0.401	2.99
ArcDD	Arc Discharge	PFDD	0.406	3.85
ArcPy	Arc Discharge	PFPy	0.396	3.21
ArcDDCz	Arc Discharge	PFDD and PCz	0.425	6.62
ArcCz	Arc Discharge	PFDD	0.452	6.30
PlaDD	Plasma	PFDD	0.405	3.79

[a)]Solution ϕ refers to the absorption peak ratios calculated from UV-Vis-NIR data.[39] Higher ϕ may qualitatively indicate higher s-CNT purity optically, however it cannot conclusively differentiate between lower band-gap CNTs and pure metallic CNTs. Hence, extensive electrical characterization of a statistically significant sample size of transistors is necessary for measuring s-CNT purity of a solution accurately.

(or PFBPy) was mixed with the PFDD/CNT film in toluene to thoroughly disperse the nanotubes by bath sonication (2h), and filtered using a PTFE membrane to collect a PFPy/CNT film. These two steps were repeated again to complete the polymer replacement. After all of the polymer-wrapped CNT samples were generated, the films were re-dispersed in toluene to undergo a set of additional conditioning treatments to further improve the s-CNT purity as well as solution stability. It was done by adding extra wrapping polymer to adjust the polymer/CNT ratio to ≈4/1 from ≈1/1 and then undergoing a 2nd hybrid process with a centrifugation (12500 rpm, 30 mins) to yield pure s-CNT solution. These pure s-CNT solutions were purged and sealed under nitrogen ambient before deposition on pre-fabricated high-k dielectric/metal gate stacks for CNFET fabrication.

Figure 1e shows the s-CNT solutions (all dispersed in toluene) used for this experiment. UV-Vis-NIR absorption spectrum for the solutions were performed using a spectrophotometer (Cary 5000, Varian) over a wavelength range from 300 to 2100 nm (Figure 2 a–c). CNT length postsorting is measured using AFM (sample AFM for laser ablated CNTs wrapped in PFDD in Figure 2d, length distributions in Figures S3–S5 in the Supporting Information).

3. Characterization

To compare the permutations and impact of CNT synthesis sources and conjugated polymers, we fabricated and electrically characterized 10 000 CNFETs for each CNT solution. Each CNFET is fabricated with a 20 µm width and contains an average of 1000 CNTs (confirmed through SEMs, **Table 2** shows further details of the transistor geometries fabricated for these measurements). Thus, a total of 10 million CNTs were measured for each CNT solution, enabling accurate extraction of s-CNT purity (see Supplemental Information for further details).

To correlate each solution with transistor quality, we measure the I_D-V_{GS} transfer characteristics of all 10 000 CNFETs per solution and extract key device metrics including on-current (I_{ON}), off-current (I_{OFF}), I_{ON}/I_{OFF} ratio and threshold voltage (V_T) (**Figure 3**,**4**). Importantly, we characterize the CNFETs with a drain bias up to V_{DS} = −1.8V in stark contrast to many prior works that characterize and claim s-CNT purity based on low V_{DS}[17,42–43] (sometimes using V_{DS} <50 mV). This distinction is critical, as grouping CNTs in two binary bins of m-CNT and. s-CNT (as is conventional in the field) leaves substantial grey area for small bandgap CNTs (Bandgap of a CNT is determined by its diameter and chirality[48]). With small V_{DS}, small bandgap CNTs can still have high I_{ON}/I_{OFF} ratio, and thus appear like s-CNTs. But at high V_{DS}, small bandgap CNTs have low I_{ON}/I_{OFF} ratios[16,44] often <10, and thus act effectively like m-CNTs within circuits. While CNFETs in circuits have a range of V_{DS} applied across them at any given time, the negative impact of m-CNTs appear primarily at high V_{DS}, and thus we pessimistically characterize our s-CNT purity similarly with a high V_{DS}, essentially classifying small bandgap CNTs as m-CNTs (as this realistically is how they negatively impact a circuit[1,50–52]).

Table 2. Transistor Parameters.

L_{CH} (µm)	1
L_G (µm)	3
L_C (µm)	3
T_{OX} (nm)	30
Width (µm)	20
L_{CH} (µm)	1
L_G (µm)	3
L_C (µm)	3

Figure 3a–i shows typical I_D-V_{GS} characteristics of a random 500 p-channel CNFET subset with channel length (L_{CH}) of 1 µm at a drain bias V_{DS} = −1.8 V (measurements at ≈23 °C) for each of the different CNT solutions (Table 1). Additionally, Figure 4f shows the cumulative distribution function (CDF) of the I_{ON}/I_{OFF} ratio as obtained from characterizing 10 000 CNFETs measured at a V_{DS} of −1.8 V. We use the CDF of I_{ON}/I_{OFF} ratios to analyze the efficacy of the solution sorting process, as solutions with higher s-CNT content would result in more transistors with higher I_{ON}/I_{OFF} ratios leading to the CDF plots shifting to the right (**Figures 5**b–d). Mean I_{ON} and I_{OFF} measured at a V_{DS} of −1.8 V extracted from I_D-V_{GS} characteristics of 10 000 CNFETs for each CNT solution is plotted as I_{ON}-I_{OFF} scatter plots (Figure 5a) with a preferred solution having a higher I_{ON} at a lower I_{OFF}.

4. Results and Discussion

From Figure 5a, we observe s-CNT solutions prepared from laser ablation CNTs outperform s-CNT solutions prepared from other CNT sources based on relative mean I_{ON} and I_{OFF}. This point is further clarified in Figure 5d which shows that CNFETs fabricated with laser ablation CNTs have an improved cumulative distribution of I_{ON}/I_{OFF} ratios (as measured from I_D-V_{GS} characteristics of ≈10 000 CNFETs at V_{DS} = −1.8 V) compared to arc discharge and plasma CNTs.

Additionally, from Figure 5c, we see that PFDD wrapped laser ablation CNTs have an improved I_{ON}/I_{OFF} ratio distribution compared to laser ablation CNTs wrapped with other polymers such as PFPy, PFBPy and PCz (s-CNT purity estimate for each solution is shown in Figure S1 and Table S1 in the Supporting Information). Figure 5b demonstrates a similar trend for arc discharge CNTs where PFDD wrapped CNTs outperform PFPy or PCz wrapped CNTs.

It is critical to note that Figure 5a–d shows how the CNT precursor and the wrapping polymer can be optimized separately for maximizing s-CNT purity. For instance, Figure 5a,d illustrates for any particular polymer, the trend in ideal CNT source selection is always laser ablation, then arc discharge, then plasma. Similarly, Figure 5b,c shows for a particular CNT source (e.g. laser ablation or arc discharge), the trend in ideal polymer selection is always PFDD, then PFPy, then PCz. These observations illustrate experimentally that the ideal CNT synthesis source and ideal polymer used for the sorting process are independent from one-another, and thus can be optimized separately.

Finally, we demonstrate how the best combination – laser ablated CNTs wrapped with PFDD achieves a s-CNT purity of 99.9953%, (an estimate of s-CNT purity is computed for each

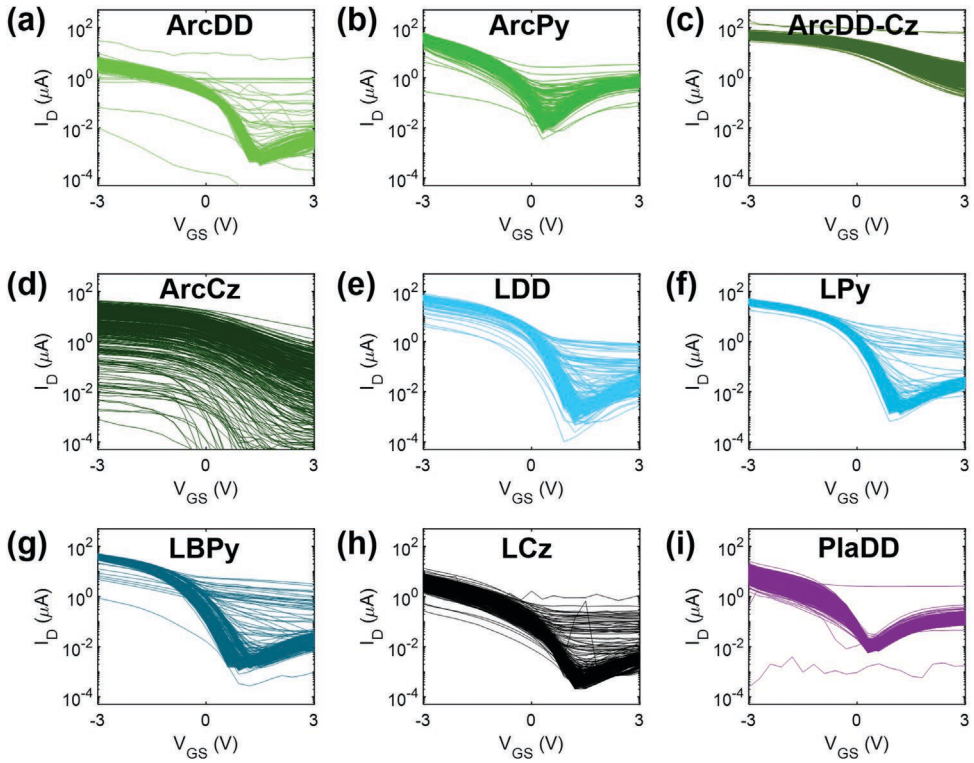

Figure 3. Typical I_D-V_{GS} characteristics of 500 CNFETs fabricated using semiconducting CNT (s-CNT) solutions extracted from different CNT sources and wrapped with different polymers: a–d) arc discharge CNTs, e–h) laser ablation CNTs, and i) plasma CNTs. Table 1 lists all the different CNT sources and polymer types. Transfer characteristics are color coded to match Figures 2, 4, and 5.

solution in Figure S1 and Table S1 in the Supporting Information), above the 99.99% threshold (as required by *DREAM* design methodology) also achieving a median on-current of ≈57 µA per FET (L_{CH} = 1 µm) and a mean I_{ON}/I_{OFF} ratio of 3×10^4 at a V_{DS} of −1.8 V. Importantly, the synthesis process for laser ablated CNTs is done at smaller scales than other techniques (e.g. arc discharge, plasma etc). Thus, future work should focus on scaling up the manufacturing process for PFDD sorted laser ablated CNTs for realizing energy efficient CNFET based digital VLSI systems.

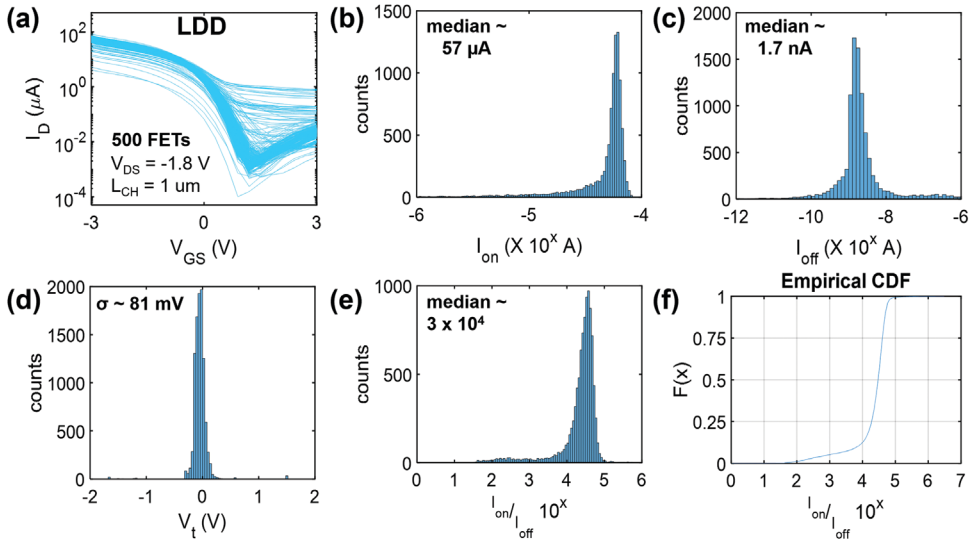

Figure 4. a) Experimental I_D-V_{GS} characteristics of 500 CNFETs measured at room temperature at V_{DS} = −1.8 V for laser ablation CNTs wrapped with PFDD. Histograms of key device metrics obtained from 10 000 CNFETs measured at V_{DS} = −1.8 V – b) I_{ON} c) I_{OFF} d) V_T and e) I_{ON}/I_{OFF} ratio. f) cumulative distribution function of I_{ON}/I_{OFF} ratio.

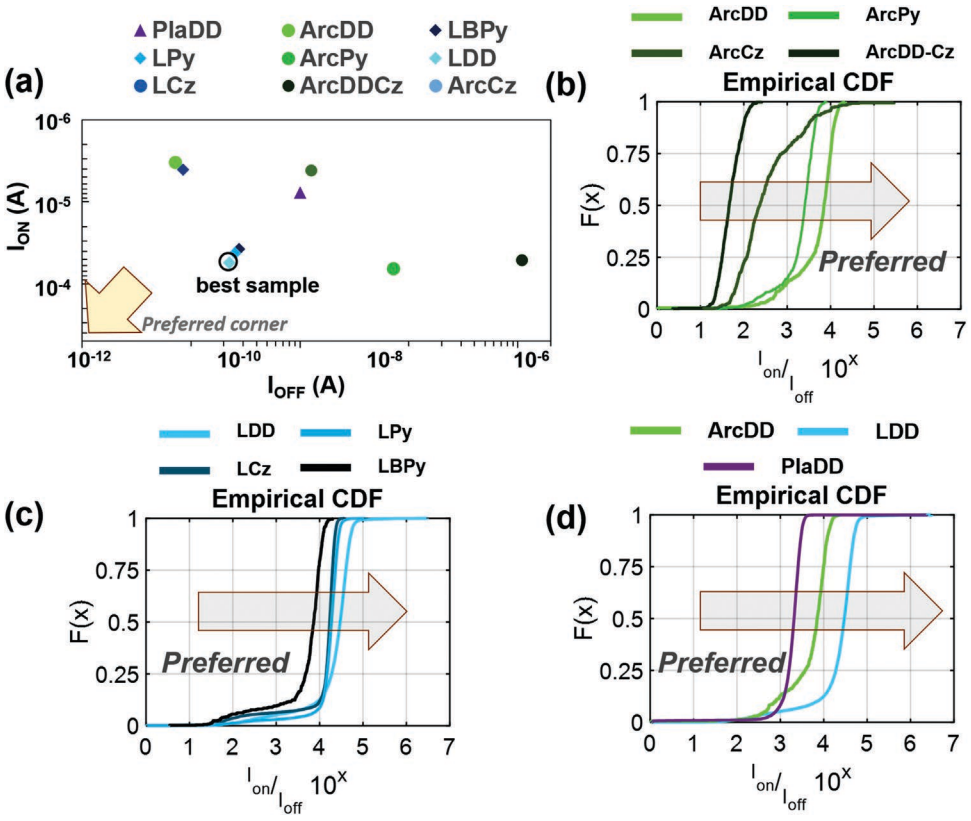

Figure 5. a) Mean I_{ON}-I_{OFF} scatter plot for each solution (listed in Table 1) – extracted from I_D-V_{GS} characteristics of 10 000 CNFETs for each solution (totaling 10 million CNTs per solution) measured at a V_{DS} of –1.8 V. All solutions are color coded to match Figures 2–4. Comparison of I_{ON}/I_{OFF} ratios for different s-CNT solutions by characterizing the cumulative distribution function of I_{ON}/I_{OFF} ratio (10 000 CNFETs per solution) for b) arc discharge CNTs wrapped with different polymers c) laser ablation CNTs wrapped with different polymers and d) PFDD wrapped laser ablation CNTs, arc discharge CNTs and plasma CNTs. All solutions are listed in Table 1.

5. Conclusion

In this work, we experimentally investigate the impact of CNT sources and polymers chosen as initial precursors for solution based conjugated polymer extraction of semiconducting CNTs on the electrical performance CNFETs by performing extensive electrical characterization of 10 000 CNFETs for each solution. Additionally, we show that the optimal polymer choice

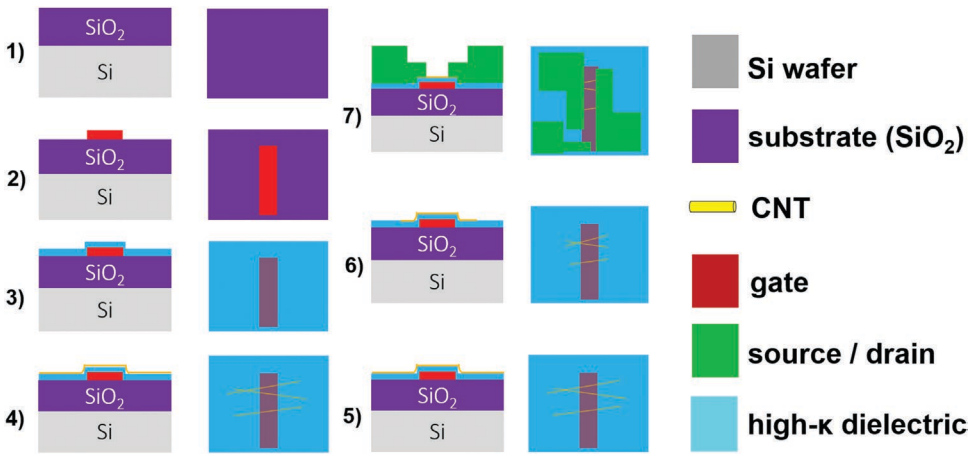

Figure 6. Process flow of back-gate CNFETs. 1) Si/SiO_2 substrate. 2) Photo lithography patterning, e-beam metal evaporation and liftoff for back-gate (2 nm Ti/ 18 nm Pt). 3) 15nm Al_2O_3 15 nm HfO_2 gate dielectric (EOT ≈ 7.5 nm). 4) Submerge die in purified semiconducting CNTs dispersed in toluene. 5) Die Clean through NMP solvent rinse. 6) Oxygen plasma etch to remove CNTs outside of transistor channel region. 7) Source/drain patterning through photo lithography patterning, e-beam metal deposition and liftoff (0.5 nm Ti/ 45 nm Pt).

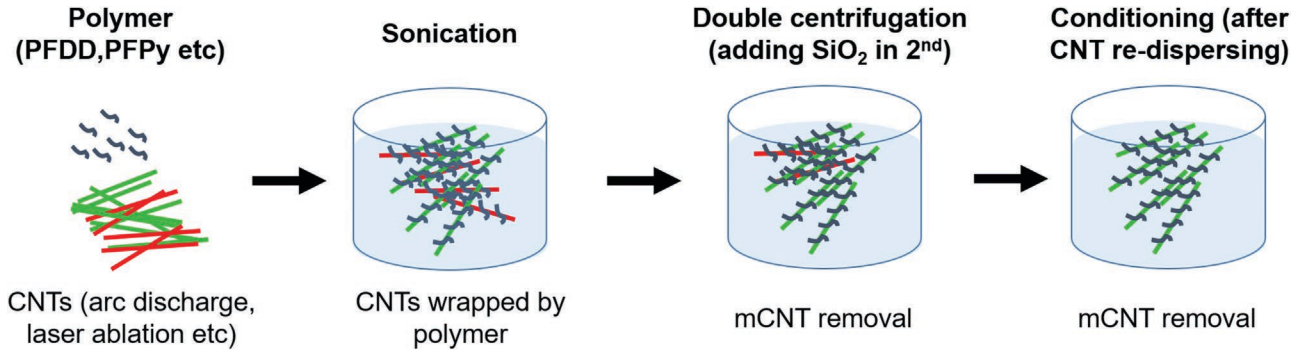

Figure 7. Enhanced hybrid conjugated polymer extraction process. a,b) Polymer and CNTs were added with toluene and tip sonicated in an ice bath for 30 min to thoroughly disperse the solid. c) The dispersion was centrifuged to obtain supernatant, which was combined with silica gel, sonicated at 30 °C for 30 min, and centrifuged again to collect the supernatant. d) The solid obtained by filtering the supernatant was re-dispersed in toluene to undergo a conditioning step to yield final solution for device fabrication.

for sorting s-CNTs is independent of the CNT source used as a precursor. Finally, we demonstrate a combination of CNT and polymer – laser ablation CNTs wrapped with PFDD polymer – that can achieve the >99.99% s-CNT purity required to realize arbitrary digital VLSI systems. Thus, this work addresses a key challenge facing CNFET-based electronics, and demonstrates a promising path toward extraction of ultra-high purity carbon nanotubes for energy efficient digital VLSI systems.

6. Experimental Section

Die Fabrication: The starting substrate for the back-gate CNFETs was silicon (resistivity of ≈100 ohm-cm) with 800 nm thermal oxide (**Figure 6**). To pattern the metal gate, the wafer was coated with a bilayer PMGI SF5 and SPR 700 photoresist (≈200 nm PMGI SF5 + 1000 nm SPR), and photolithography (with a Heidelberg maskless aligner) was used to define the gate electrode. Exposed photoresist was developed at room temperature (≈21°C) using CD-26. Electron beam (ebeam) evaporation is used to deposit 20 Å of Titanium followed by 18 nm Platinum, followed by lift-off. Atomic layer deposition (ALD) was used to deposit 15 nm Al_2O_3 followed by 15 nm high-k HfO_2[53] over the gate metal at 200°C. Following gate-stack fabrication, photolithography was performed using positive photoresist SPR to pattern contact holes to the gate metal electrodes, and a dry Cl_2-based plasma etch was used to etch through the HfO_2. The SPR was stripped in acetone, followed by oxygen plasma. To prepare the wafer for CNT deposition, the surface was functionalized with hexamethyldisilazane (HMDS). The wafer was then submerged in s-CNT solutions of toluene (CNT incubation[40]) containing >99.9% pure semiconducting CNTs (modified Nanointegris[37] and NRC supplied sCNT solutions) for 48 h. To make the deposition uniform and reproducible a CNT concentration of 2 µg ml^{-1} was used for the deposition. After CNT incubation, a solvent cleaning step (coat pieces in PMGI SF5, bake at 235 °C and sonicate pieces in NMP) was performed to remove CNT aggregates from the surface of the die (RINSE[1]). After RINSE, SPR was patterned to cover the transistor channel regions, and oxygen plasma removed all excess CNTs (outside the channel region). Finally, the source and drain (5 Å Ti/ 45 nm Pt) were defined and patterned similar to the gate electrode.

Conjugated Polymer Extraction Process: The sc-SWCNTs solutions of laser (L), plasma (Pla) and arc-discharge (Arc) tubes were prepared using an enhanced h-CPE (eh-CPE) process (**Figure 7**) which include a traditional hybrid conjugated polymer extraction (h-CPE),[39,49] and then a final conditioning treatment. The eh-CPE process was started by mixing 160 mg of acid treated raw SWCNTs sample with 128 mg of PFDD (or, PCz) in 200 ml toluene. The mixture was sonicated for 30 min in an ice bath using a tip sonicator (Branson sonifier 250, 200 W maximum power) with a 10 mm tip operated at 60% duty cycle and 70% output. This process was repeated once again to the sediment. The supernatant of the second extraction was mixed with 200 mg of silica gel, sonicated in a bath sonicator (Branson 2510 sonicator) at ≈30°C for 40 min, stored overnight, and then centrifuged at 12 500 rpm (SLA1500 rotor, RCF:23700g) for 30 min. Afterward, the extracted solution was filtered using a 200 nm PTFE membrane to collect PFDD/CNTs as a black film with a polymer to CNT weight ratio (P/CNT ratio) of ≈1/1. For the samples with the wrapping polymer other than PFDD (or, PCz), a polymer exchange step was added. As an example, for a PFPy/CNT sample it was done by mixing 6 mg of a PFDD/CNT film with 30 mg of PFPy in 100 mL of toluene. This solution was then bath sonicated for 2 h and filtered to collect a PFPy/CNT film. This process was repeated once again to complete the polymer replacement. At last, 4–6 mg of each polymer wrapped CNT film (either obtained through direct extraction, or through polymer exchange) was dissolved in 100 mL toluene, and then underwent a conditioning to obtain the final solution with an enhanced s-CNT purity and solution stability. It was done by mixing each polymer wrapped CNT sample with more of the same polymer to adjust the P/CNT ratio in between 3/1 to 5/1 (initially, P/CNT ratio was 1/1) and then bath sonicating the solutions for 3 h at 30°C. Then the solution was underwent a hybrid process again with a final centrifugation to complete the conditioning treatment. These pure s-CNT solutions were purged and sealed under nitrogen before deposition on high-k/metal gate stacks for CNFET fabrication.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Data Availability Statement

The data that support the findings of this study are available from the corresponding author upon reasonable request.

Keywords

carbon nanotubes, FETs, carbon nanotube FETs, nanomaterials

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