Simulation of digital control systems on an analog computer with digital logic
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SIMULATION OF DIGITAL CONTROL SYSTEMS ON AN ANALOG COMPUTER WITH DIGITAL LOGIC

- C. R. CLEMENCE -

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ABSTRACT

A procedure for simulation of digital control systems is described which uses a simple hybrid arrangement consisting of the conventional elements of an analog computer and the digital elements normally provided in the digital panel available as an accessory from most analog computer manufacturers. The method is developed from the basic principles of the z-transform and the zero-order hold, and applied to the synthesis of suitable software compensation for a variety of control problems including some with non-uniform sampling characteristics. In each case, the response of the simulated system is compared with a calculated response to confirm the accuracy and validity of the simulation.

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SIMULATION OF DIGITAL CONTROL SYSTEMS ON

AN ANALOG COMPUTER WITH DIGITAL LOGIC

— C. R. Clemence —

Introduction

In the last few years, digital computers have become increasingly important as controlling elements in closed-loop control systems, and with the presently available speed and capacity, it is practical to control very complex systems or to have one computer control many systems. With digital techniques, control synthesis differs from that of continuous data systems because the signals must appear as samples or pulses, and delays will be encountered due to finite computing times or time-sharing of computer facilities. Since any delay usually tends to create instability, the theory of stabilization of this type of system has been well developed and many control loops of various degrees of complexity are now in existence. Because of uncertainties in regard to the physical characteristics such as inertia, friction, orifice flow, heat transfer, etc., of the devices being employed, the design procedure for all but the very elementary system calls for a simulation and the setting up of stability criteria tailored to the expected variation of the uncertain characteristics. Digital computers have many advantages for data processing and the performance of routine calculations, but are, in general not well suited to this type of simulation because the digital program is usually an artificial sequence of steps which bear little relation to the physical processes involved. On the other hand, the analog computer can provide real-time (or time-scaled) solutions to the differential equations and a "live-model" presentation which makes it eminently suitable for representing the continuous-data part of a proposed system. The purpose of this paper is to show that the modern analog computer can be adapted to represent the digital part also, in a manner which allows the engineer to manipulate the software by changing digital parameters or introducing new sampling rates, to determine the effects of computer speed or of time-sharing, and often to make a significant improvement in the system response by calibrated potentiometer adjustment while observing the result on an oscilloscope display. Since one of the problems in simulation is to confirm that the simulation truly represents the device being simulated, theoretical calculations will be made in parallel and comparison of mathematical and simulation results will be provided throughout.

Simulation Requirements

The simulation of digital software has been made possible by the recent introduction of digital logic as an analog computer accessory. This circuitry has been designed by the computer manufacturers primarily for the purpose of manipulating analog parameters in a purely analog representation of a problem, but it can be easily adapted to control of the computer elements in a manner which will produce a simulation of digital-control software.
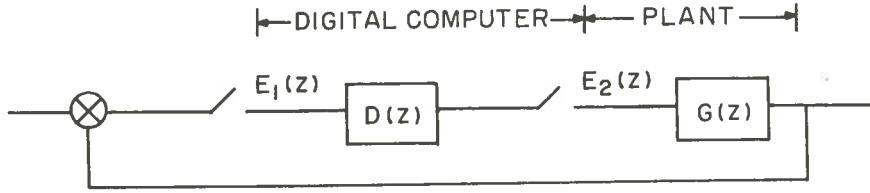
Figure 1   Block diagram of a digital control system

The methods to be used may be derived from a consideration of the software character-istics. Since the digital calculation is based on pulses (samples), the pulse transfer function of any dynamic process (the 'plant' in Fig. 1) can be stated as a z-transform, thus

$$G(z) = G*(s) \Big|_{z = e^{sT}} \qquad \text{where } T \text{ is the sampling interval}$$

$$= \frac{a_0 + a_1 z^{-1} + a_2 z^{-2} + \dots}{1 + b_1 z^{-1} + b_2 z^{-2} + \dots} \tag{1}$$

To produce any desired output such as a least-squared error, ripple-free response, or zero steady-state error, sampled data theory shows that the controlling element, $D(z)$, must have a transfer function of the form

$$D(z) = \frac{E_2(z)}{E_1(z)} = \frac{c_0 + c_1 z^{-1} + c_2 z^{-2} + \dots}{1 + d_1 z^{-1} + d_2 z^{-2} + \dots} \tag{2}$$

Placing $e^{sT} = z$ and converting (2) to the time domain

$$E_2(t) = c_0 E_1(t) + c_1 E_1(t - T) + c_2 E_1(t - 2T) + \dots$$
$$- [d_1 E_2(t - T) + d_2 E_2(t - 2T) + \dots] \tag{3}$$

Equation (3) shows that the digital software is based upon a manipulation of present and past samples and so requires memory capacity and an arithmetic capability. It is apparent also that the simulation requires a timing system to produce the sampling interval and to provide delays such as may be found in the real system. These require-ments can be met by appropriate use of analog computing elements controlled by the digital logic in the manner to be described.

Operations of Sample, Hold and Delay

Ignoring the arithmetic operations for the moment, the fundamental operations of a control device, $D(z)$ of Fig. 1 as represented by Equation (2), are to sample, to hold, and to delay. It is appropriate to discuss these concepts briefly and also some basic principles of the z-transform which are most pertinent to the simulation methods to be developed. The sampling of any analog signal can be described mathematically as the product of a train of unit impulses, and analog information, as shown in the curves A
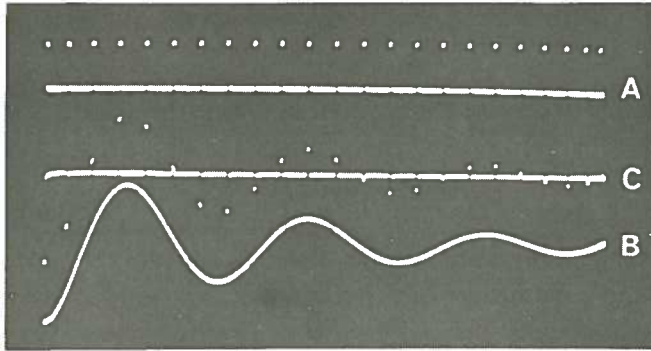
Figure 2 Sampling of an analog signal A – Unit pulse train;
B – Analog signal; C – Product of A and B

and B respectively of Fig. 2. The curve C, obtained by an analog multiplier, is the product thus

$$R^*(t) \;=\; R(t) \sum_{n=-\infty}^{+\infty} \delta(t - nT) \quad \text{where } T = \text{the sampling interval} \qquad (4)$$

Because of the nature of hardware it is often necessary to keep the sample available for a short period of time. In the digital process, a memory store is used while, in the analog, the integrator 'hold' mode can be utilized to store the value at the instant of sampling until the next sample is available. This is called a zero-order hold and is illustrated in Fig. 3. The modulated pulses, A, after passing through a sampling device and zero order hold are shown in curve B. The curve C is produced when curve B is passed through another device producing a delay of T, one sampling interval.
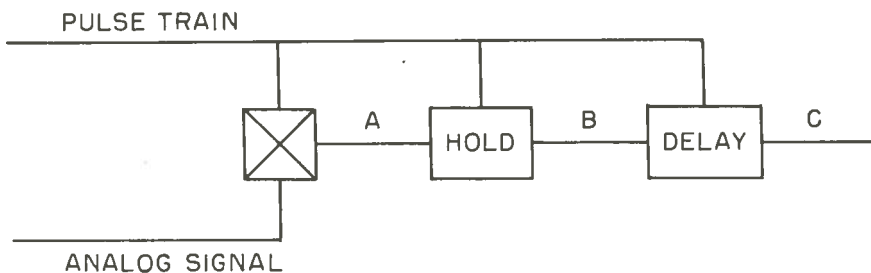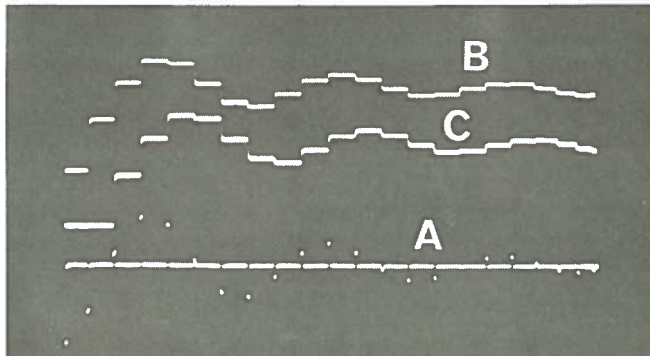

Figure 3 Example of zero-order hold and one sampling interval delay.
Curves A, B and C are taken from points A, B and C, respectively, on the diagram.

Implementation of Sample, Hold and Delay

It is now appropriate to discuss the manner in which the sampling, zero-order hold, and the delay can be mechanized on an analog computer with digital logic. A number of methods have been proposed [1, 2] which usually require very short and accurate sampling pulses in order that one amplifier only may perform both the sample and hold functions, but which may accumulate appreciable timing errors as the sample is given successive delays as required for implementation of Equation (3).

In order to utilize low-cost units and to simplify the timing requirements, a method of switching the sample-hold devices using square waves rather than short pulses has been used. (Hereafter these devices will be called "track-hold" as being more appropriate since each one "tracks" on one half cycle of the square wave and "holds" on the other half). This method requires two track-hold devices, acting as a pair, to simulate each sample-hold operation and each delay. The modes of operation and the connections of the amplifier-integrators to obtain the track-hold functions are illustrated in Fig. 4. Note that the first pair provides a sample-hold only, while the second pair provides a delay equal to one cycle of the square wave.

*Figure 4 Operation of two track-hold pairs in tandem
to produce a sample, hold and delay function.*

Thus the sampling frequency is equal to that of the square wave and the instant of sampling occurs when the second unit of any pair is switched to "track". This method requires more analog equipment than the single amplifier method but sampling errors, timing errors, and other equipment problems are virtually eliminated and logic hardware requirements are simplified considerably. Note also that, although the hold operation precedes the delay in this case, the effect is the same as it would be if the delay were preceding the hold.

The additional amplifiers necessary for this method are not a serious disadvantage since sample-hold units are now readily available at quite reasonable cost, or, in any problem set-up, there is likely to be a number of unused amplifier-integrators in the computer.

Digital Logic

As will be seen in the diagrams to follow, the digital logic consists of pulse generators (clocks), flip-flops, variable monostable multivibrators, and some AND and OR gates. All of these items are generally included in the accessory digital logic but, if not, they are available commercially in modular form usually directly compatible with the computer to be controlled.

Principles of z-Transforms

Sampled data theory and the z-transform are very well developed in a number of textbooks [3, 4, 5] some of which are listed in the references, so that no general outline need be given here. However it may be useful to discuss very briefly the unit step, the zero order hold, and the unit ramp to provide some background for later calculations and to indicate the inherent simplicity of the z-transform approach.

(a) The Unit Step Function

It has been noted above (Equation 4) that a modulated train of impulses may be represented as:

$$R^*(t) = R(t) \sum_{n=-\infty}^{+\infty} \delta(t - nT) \qquad \text{where } T \text{ is the sampling interval}$$

The Laplace transform of this is the 'pulse transfer function':

$$R^*(s) = R(s) \sum_{n=-\infty}^{+\infty} e^{-nTs} \tag{5}$$

Then, for unit impulses starting at $t = 0$

$$R*(s) = (1) \sum_{n=0}^{+\infty} e^{-nTs}$$

$$= 1 + e^{-Ts} + e^{-2Ts} + e^{-3Ts} + \cdots$$

$$= \frac{1}{1 - e^{-Ts}} \tag{6}$$

Note that equation (6) is also the Laplace transform of a unit step function which has been sampled at intervals of T. For ease of manipulation, a substitution of $z = e^{sT}$ has been made so that for a step,

$$R(z) = \frac{1}{1 - z^{-1}} = \frac{z}{z - 1} \tag{7}$$

which is known as the z-transform of a unit step function. Thus the z-transform of any time function, $R(t)$, is the same as the Laplace transform of $R*(t)$ with the change of $z = e^{sT}$ as indicated.

(b) Zero-order Hold

The Laplace transform of the zero-order hold is, of course, simply the transform of a rectangular pulse of unit amplitude and length T,

$$L[1(t) - 1(t - T)] = \frac{1}{s} - \frac{e^{-sT}}{s}$$

$$= \frac{1 - e^{-sT}}{s}$$

$$= \frac{1 - z^{-1}}{s} \tag{8}$$

(c) The Unit Ramp

The unit ramp is often used as a test signal and is defined as that function which increases by one unit per unit of time. The pulse transfer function is:

$$R*(s) = \sum_{n=0}^{+\infty} nT e^{-nTs}$$

$$= 0 + T e^{-Ts} + 2T e^{-2Ts} + 3T e^{-3Ts} + \cdots$$

This may be thought of as the product of two transfer functions, a step of amplitude T, and a unit step delayed by T. The product is:

$$\frac{T}{1 - e^{-sT}} \times \frac{e^{-sT}}{1 - e^{-sT}} = \frac{T e^{-sT}}{(1 - e^{-sT})^2}$$

$$= \frac{T z^{-1}}{(1 - z^{-1})^2} = \frac{T z}{(z - 1)^2} \qquad (9)$$

(d) Other Time Functions

The transforms of a number of time functions are listed in tables or may be derived as required. For example, transforms of $K(1 - e^{-at})$ are as follows:

The Laplace transform is: $\quad L [K(1 - e^{-at})] = K \dfrac{a}{s(s + a)}$

and the z-transform is: $\quad Z [K(1 - e^{-at})] = K \dfrac{(1 - e^{-aT})z}{(z - 1)(z - e^{-aT})}$

where T is the sampling interval as before.

Illustrative Example

A block diagram of a simple system is shown in Fig. 5 (a) where the first sampler may be an analog-digital converter, the gain K and the second sampler represent the digital computer and $G_1(s) = \dfrac{a}{s(s + a)}$ represents the plant. A 'hold' circuit is placed between the computer and the plant because the latter is a 'continuous-data' device such as a D.C. motor and does not operate well on samples. Such a system may be simulated as shown in Fig. 5 (b) in which one track-hold pair, T-H-1, and the potentiometer, K, are used for the digital computer and the hold, while the plant is represented in analog form. That this is a true simulation can be readily verified by calculation of the output and comparison with the output of the simulated system. To do this, take the z-transform of the computer, the hold circuit, and the plant, as

$$Z [K, G_{ho}, G_1(s)] = Z [K \frac{1 - e^{-sT}}{s} \frac{a}{s(s+a)}]$$

$$= K \left[\frac{T z^{-1}}{1 - z^{-1}} - \frac{1}{a} \frac{(1 - e^{-aT}) z^{-1}}{1 - e^{-aT} z^{-1}} \right]$$

$$= \frac{0.424 z^{-1} + 0.364 z^{-2}}{(1 - z^{-1})(1 - 0.606 z^{-1})} \qquad (10)$$

where $a = 25$, $T = 0.02$, $K = 100$.
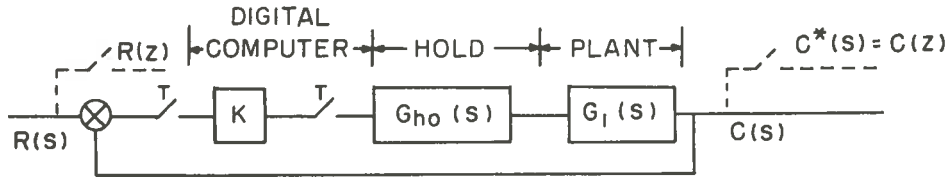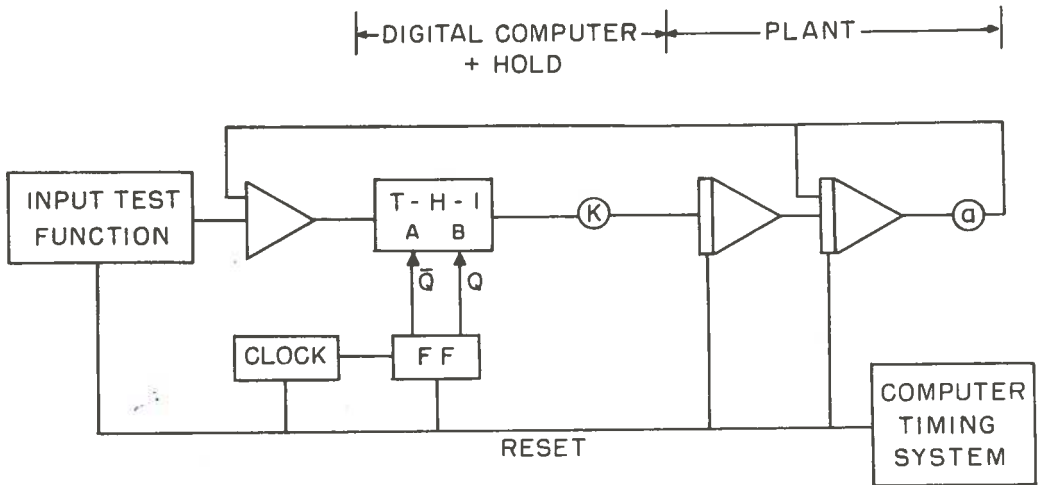
Figure 5 A simple digital control system
(a) Block diagram; (b) Simulation diagram

Also,

$$C(z) = \frac{K\,G_{ho}\,G_1(z)}{1 + K\,G_{ho}\,G_1(z)}\;R(z) \qquad (11)$$

For a step position input: $R(z) = \dfrac{1}{1 - z^{-1}}$ and, using the results calculated in Appendix A:

$$C(z) = 0.42\,z^{-1} + 1.29\,z^{-2} + 1.90\,z^{-3} + 1.78\,z^{-4} + 1.07\,z^{-5} + \ldots$$

Note the agreement of these figures with the values of the samples shown on the photograph in Fig. 6 which contains oscilloscope traces of the output, $C(t)$, and the output samples, $C(z)$, with a hold circuit applied to delineate the sample values.
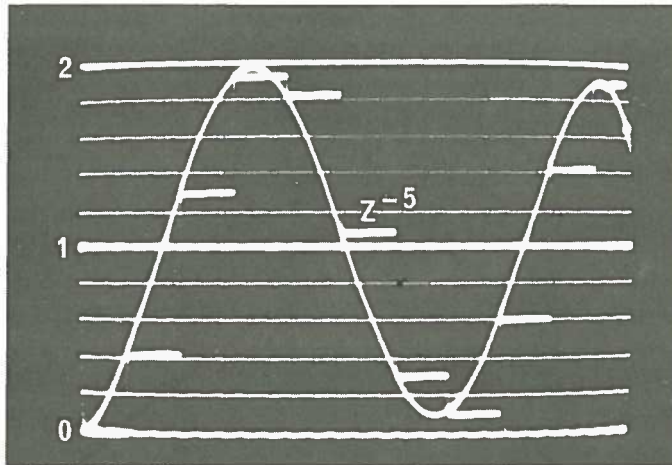
Figure 6 Unit step-response of simple digital system

$$C(z) = 0.42\, z^{-1} + 1.29\, z^{-2} + 1.90\, z^{-3} + 1.78\, z^{-4} + 1.07\, z^{-5} + \ldots$$

Minimal Prototype[†] Design

It is evident that the response shown in Fig. 6 is too oscillatory to be practical. The transfer function of a system having minimal prototype response to a step input is defined to be

$$K(z) = \frac{C(z)}{R(z)} = z^{-1} \tag{12}$$

for a transient response of one sampling interval.

Equation (11) may be rewritten to include a digital compensation function, $D(z)$, so that:

$$C(z) = \frac{D(z)\ K\ G_{ho}\ G_1(z)}{1 + D(z)\ K\, G_{ho}\ G_1(z)}\ R(z)$$

and, re-arranging

$$D(z) = \frac{1}{K\, G_{ho}\ G_1(z)}\ \frac{K(z)}{1 - K(z)} \tag{13}$$

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† Minimal Prototype Design requirements for a step input are, in brief:

(a) Steady-state response to be zero.

(b) Transient response to be in minimum time.

(c) Settling time to be finite.

Substituting equations (10) and (12) in (13)

$$D(z) = \frac{2.36 - 1.43\,z^{-1}}{1 + 0.86\,z^{-1}} \qquad (14)$$

and using the form of equation (3)

$$E_2(t) = 2.36\,E_1(t) - 1.43\,E_1(t-T) - 0.86\,E_2(t-T)$$

where E_1 and E_2 are the input and output, respectively, of $D(z)$, when converted to the time domain. Equation (14) may be represented by a digital flow diagram as shown in Fig. 7(a) which, in turn, may be simulated as shown in Fig. 7(b). As indicated above, the first track-hold (T-H-1) performs the "sample" and "hold" operation of the flow diagram and does not create any sample delay while T-H-2 and T-H-3 each provide a delay of one sampling interval. Once again the calculated output for a step input may be compared with the actual output of the simulated system (Fig. 7(c)) to confirm the accuracy of the calculations and the validity of the simulation. The calculated output, using equation (12) is:

$$C(z) = K(z)\ R(z)$$
$$= z^{-1} \times \frac{1}{1 - z^{-1}}$$
$$= z^{-1} + z^{-2} + z^{-3} + \ldots \qquad (15)$$

which means that the output must have zero error at every sampling instant after $t = 0$. This is shown to agree with the simulated output (Fig. 8) where the sampling instants are indicated by the zero crossings of a super-imposed rectangular wave. This is an ideal response so far as the computer is concerned since the output of the plant at every sampling instant has no error and satisfies equation (15) exactly. However the intersample error (called "ripple") is very large, and would remain undetected without use of an analog simulation such as described or use of a digital computer program utilizing partial delays. Note the clear picture of the response obtained by analog means.
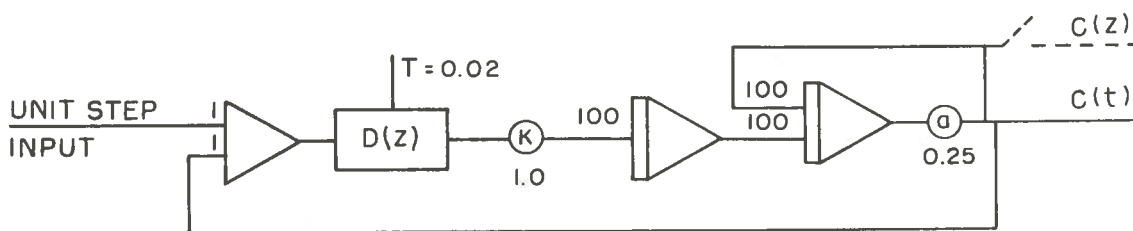
Ripple-Free Systems

Methods are available for design of ripple-free systems which reach steady-state in a minimum number of sampling intervals. A digital program for the system discussed above which will produce a ripple-free response to either a step or ramp input can be designed.
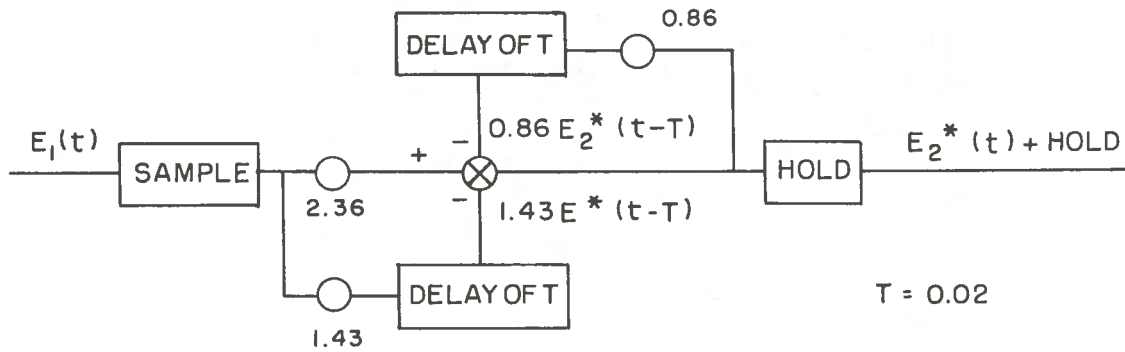
(a)
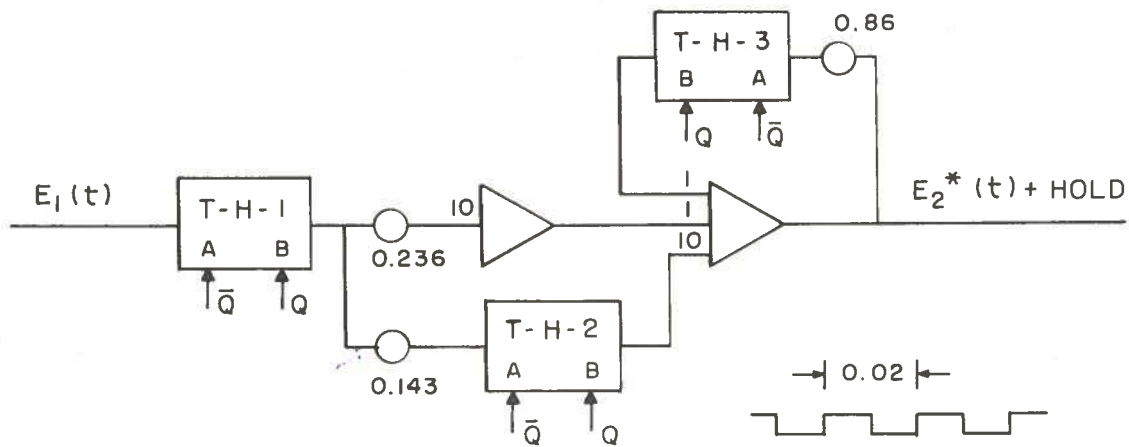
(b)

(c)

Figure 7 (a) Digital flow diagram for D(z) of Equation (14)
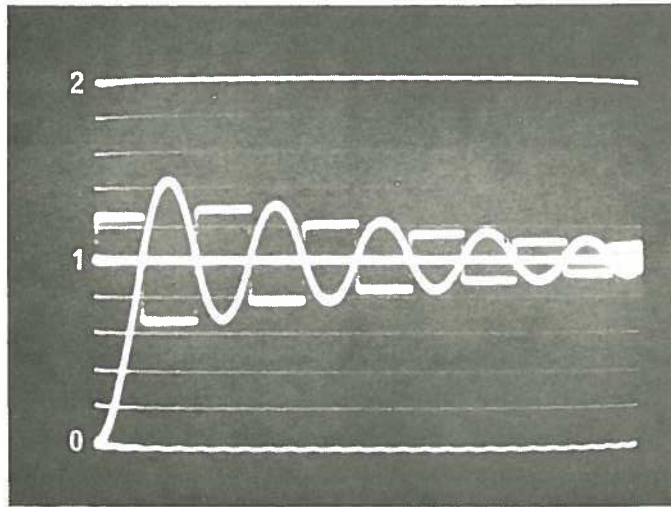*(b) Simulation of D(z); (c) Complete system*

*Figure 8 Minimal prototype response to a
unit step input for the system of Figure 7*

Calculations are given in Appendix B and result in a digital compensator with the transfer
function

$$D(z) = \frac{3.123 - 3.745\,z^{-1} + 1.123\,z^{-2}}{1 - 0.324\,z^{-1} - 0.676\,z^{-2}} \tag{16}$$

Then, using the form of equation (3)

$$E_2(t) = 3.123\,E_1(t) - 3.745\,E_1(t-T) + 1.123\,E_1(t-2T)$$

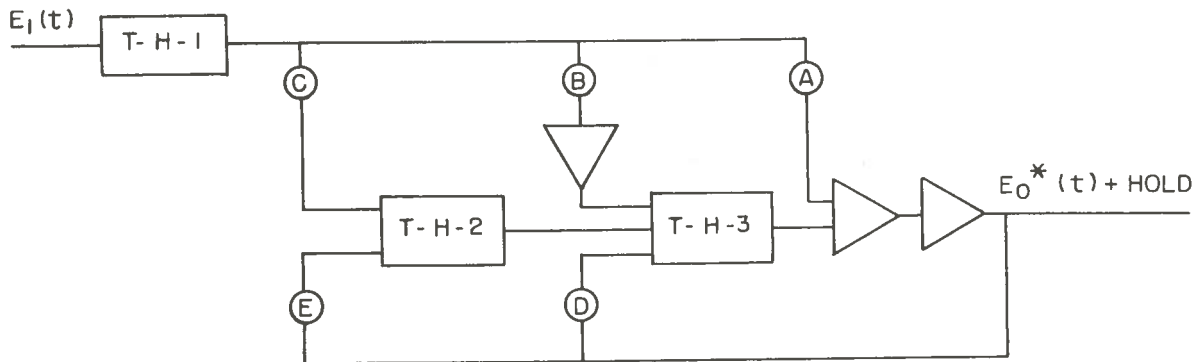$$+ 0.324\,E_2(t-T) + 0.676\,E_2(t-2T) \tag{17}$$

which can be simulated by one of the methods shown in Fig. 9. The responses to a step
and a ramp are shown in Fig 10 (a) and (b) respectively. To confirm the simulation,
the values of the response curves at the sampling instants may be compared with the
calculated values which are obtained using equation (3) in Appendix B.
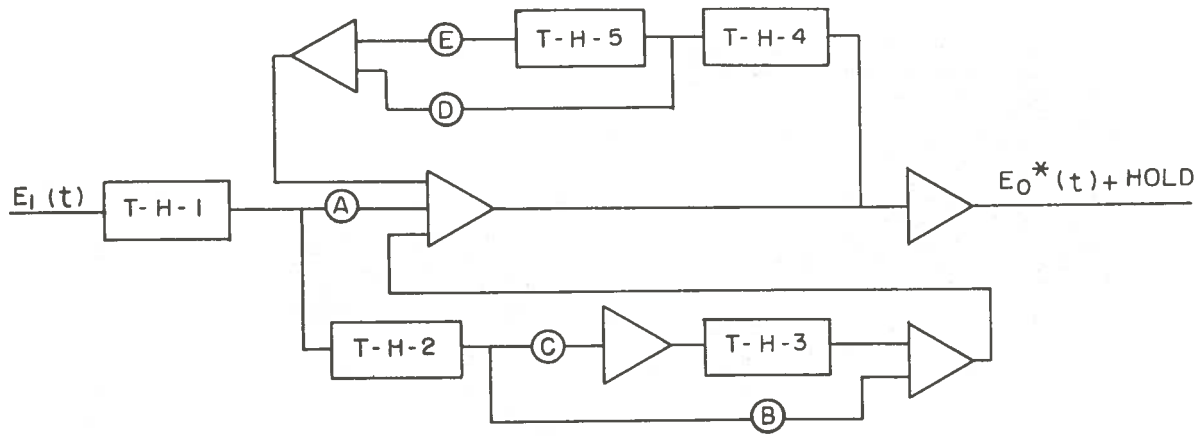
(a)
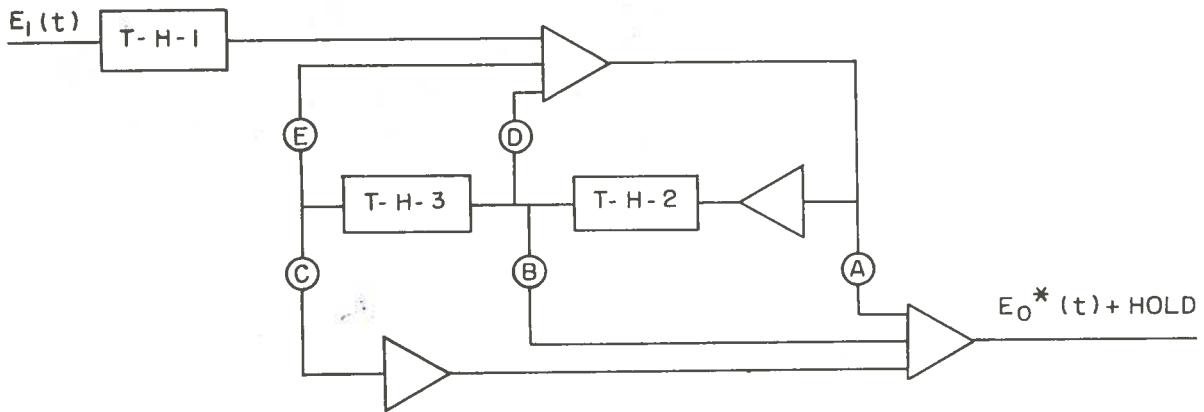
(b)

(c)

Figure 9 Three methods of simulating a digital controller transfer function such as

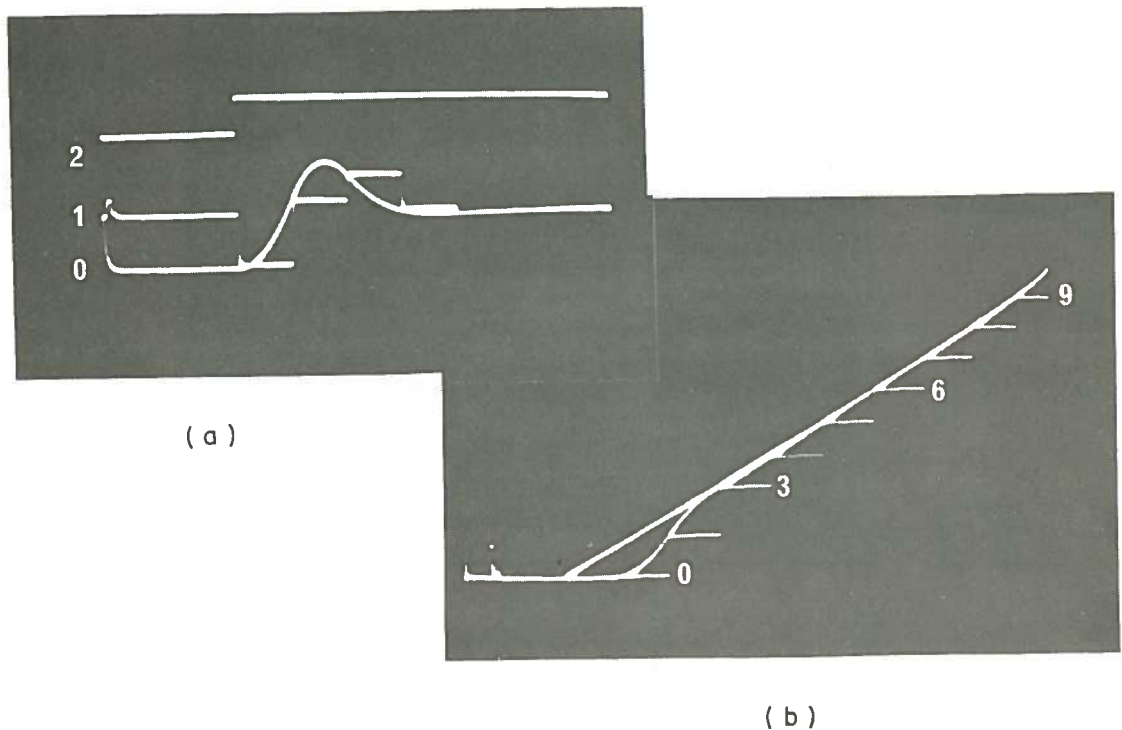$$D(z) = \frac{A - B\,z^{-1} + C\,z^{-2}}{1 - D\,z^{-1} - E\,z^{-2}}$$

(a)

(b)

Figure 10 Responses of the system of Figure 7(c) with digital compensation of Equation (16)
(a) Step Response $C(z) = 1.32\, z^{-1} + 1.68\, z^{-2} + 1.00\, z^{-3} + 1.00\, z^{-4} + \ldots$
(b) Ramp Response $C(z) = 1.32\, z^{-2} + 3.00\, z^{-3} + 4.00\, z^{-4} + 5.00\, z^{-5} + \ldots$

$$C(z)\,(step) \;=\; K(z)\, R(z)\,(step)$$

$$= (1.324\, z^{-1} + 0.353\, z^{-2} - 0.674\, z^{-3})\, \frac{1}{1 - z^{-1}}$$

$$= 1.32\, z^{-1} + 1.68\, z^{-2} + 1.00\, z^{-3} + 1.00\, z^{-4} + \ldots \quad (18)$$

and for the ramp input

$$C(z)\,(ramp) \;=\; K(z)\, R(z)\,(ramp)$$

$$= (1.324\, z^{-1} + 0.353\, z^{-2} - 0.674\, z^{-3})\, \frac{z^{-1}}{(1 - z^{-1})^2}$$

$$= 1.32\, z^{-2} + 3.00\, z^{-3} + 4.00\, z^{-4} + 5.00\, z^{-5} + \ldots \quad (19)$$

In the photographs, the $C(z)$ output (obtained by a sample-hold) is super-imposed on the $C(t)$ output to indicate the output sample values. (The first sample, z^0, is at the beginning of the step and the ramp in each case).

Computer Delay

So far, no account has been taken of the delay contributed by the finite computing time required by the computer to complete the software program. In most cases, this delay is negligible but, if not, it may be simulated by inserting an extra track-hold device as shown in Fig. 11(a) with its mode controlled by a monostable circuit which is, in turn, controlled by the primary sampling wave. The effect is illustrated in the accompanying photograph Fig. 11 (b).
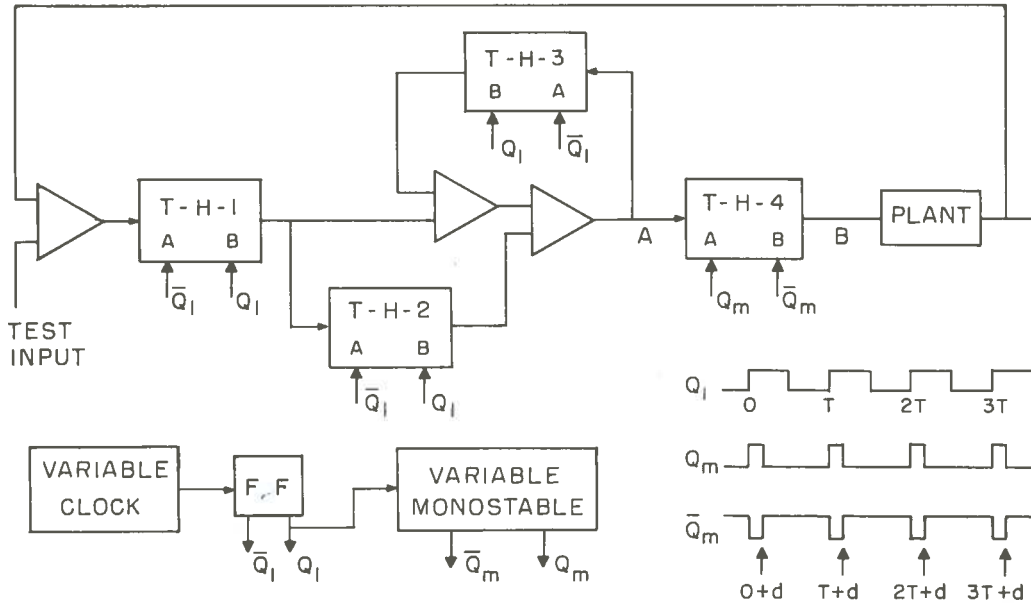
(a)
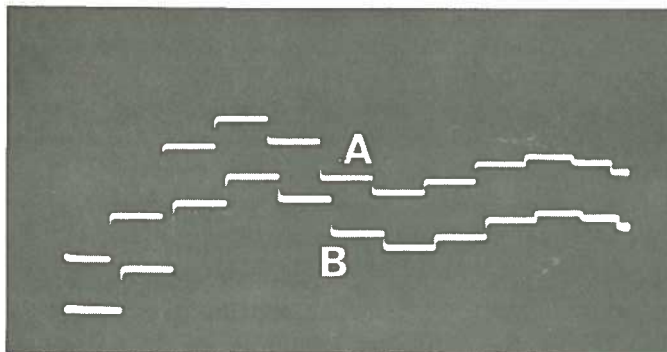
(b)

Figure 11 (a) Simulation of computer delay by adding one more track-hold pair (T-H-4); (b) Time relationship of points A and B of (a).

The same procedure can be used to simulate sampling delay (or dead time) such as might be caused by the time required to analyze output of the plant. One method of simulating a delay in the feedback is shown in Fig. 12.
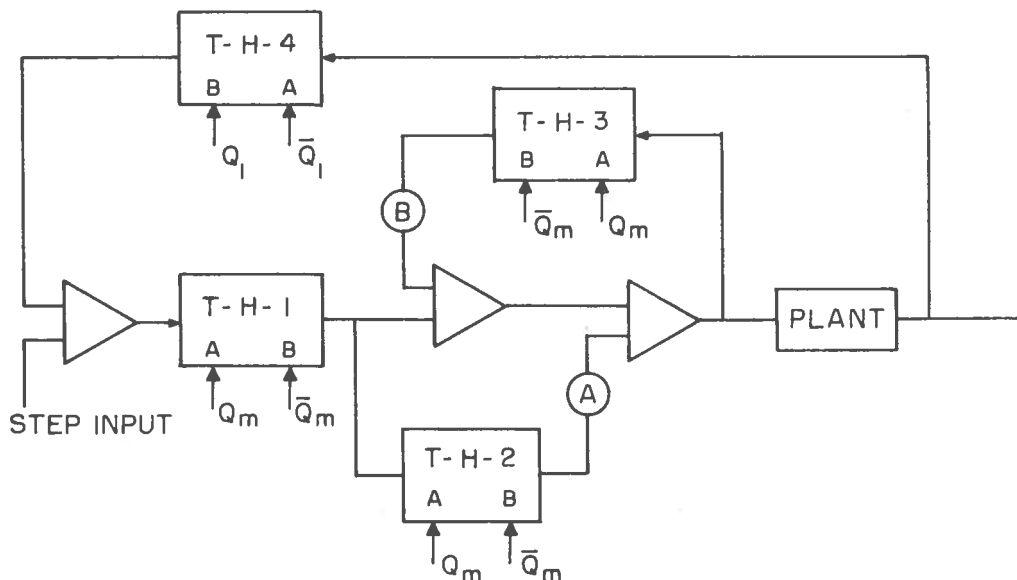

Figure 12 Feedback sampling delay (step input only) (Q_1, $\overline{Q}_1$, Q_m and $\overline{Q}_m$ have time relationships as given in Figure 11 (a)).
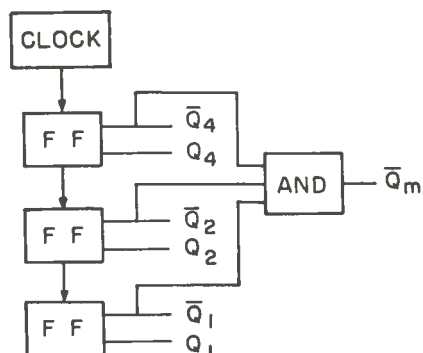
Multi-Rate Sampling

It has been found that the methods described above are also applicable to the simulation of multi-rate systems. A situation which commonly occurs is one in which the error sampling interval is fixed by physical considerations of the plant but additional time is available on the digital controller. An example is shown diagrammatically in Fig. 13 (a) where the error has been sampled at interval T but $D(z_n)$ operates with a computing interval of T/n (n is an integer) and supplies output samples to the plant at the new (faster) rate. The circuit diagram of the simulation, which follows the pattern of Fig. 9 (b) is given in Fig. 13 (b) with a table of controller constants (see calculations in Appendix C) required to obtain minimal prototype response to a ramp input. (The error at the sampling instants must be zero). The method of generating the required track-hold waveforms using the digital logic is shown in Fig. 13 (c) and the outputs, $\overline{Q}_m$, Q_1, Q_2 and Q_4 are shown as traces A, B, C, and D respectively of Fig. 13 (d). The corresponding responses of the simulated system are given as traces E, F and G for $n = 1$, 2 and 4 respectively, and are seen to have the "zero error at sampling instants" characteristic as required. The "gate" in the error path, Fig. 3 (b), controlled by $\overline{Q}_m$, is necessary because the mathematical model requires that when the controller operates at a faster rate, input at those new sampling instants which do not coincide with the

(a)

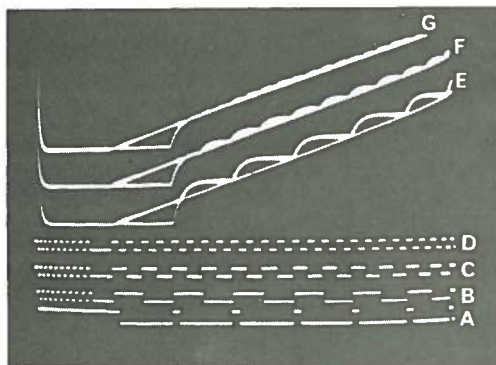|	n = 1	n = 2	n = 4
A	2.00	1.55	1.52
B	1.00	1.08	1.49
C	0.00	0.03	0.22
D	2.00	2.00	2.00
E	1.00	1.00	1.00
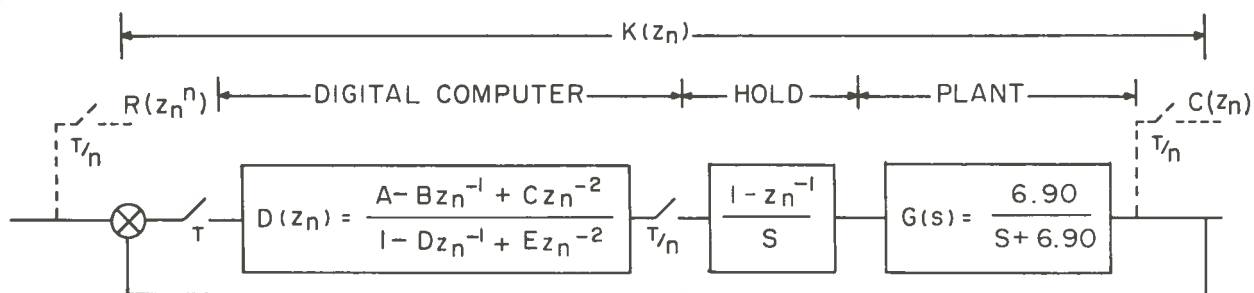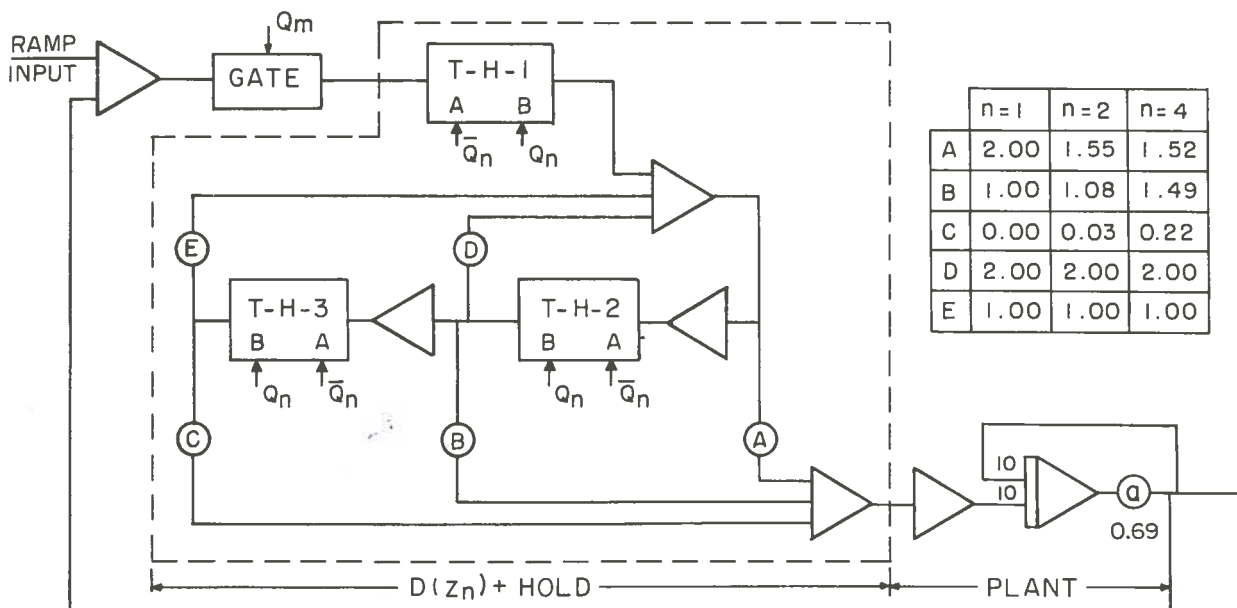
(b)

(c)

(d)

Figure 13 (a) Two rate digital control system; (b) Simulation circuit diagram;
(c) Digital logic required to generate sampling waveforms;
(d) Ramp responses and sampling waveforms for n = 1, 2, and 4. (see text).

original (slow) sampling instants, must be zero. This is obtained by gating the error signal at the slow rate so that its value is zero except when required. The mathematical model could, of course, have been altered to suit but this results in a more complicated calculation without improving the simulation demonstration. The simulation may be verified by calculating the series expansion of any of the step or ramp outputs using

$$C(z_n) = K(z_n) R(z_n{}^n) \tag{20}$$

For example, when $n = 2$, $K(z_n)$ is given in equation (2) of Appendix C, and the input is a ramp

$$C(z_2) = \left[\frac{1 - z_2{}^{-2}}{1 - z_2{}^{-1}} \right]^2 \left[1.5 z_2{}^{-1} - z_2{}^{-2} \right] \frac{z_2{}^{-2}}{(1 - z_2{}^{-2})^2}$$

$$= \frac{1.5 z_2{}^{-3} - z_2{}^{-4}}{(1 - z_2{}^{-1})^2}$$

$$= 1.5 z_2{}^{-3} + 2.0 z_2{}^{-4} + 2.5 z_2{}^{-5} + \ldots \tag{21}$$

which agrees with the simulation result given in Trace F in Fig. 13 (d).

A Two-Plant Two-Rate System

Another type of multi-rate problem may occur when two or more analog devices (plants) with different sampling rates are in cascade or one plant is in the forward loop and one in the feedback loop. Such systems are illustrated diagrammatically in Fig. 14 (a) and (b) with the simulation diagram shown in 14 (c). The simulation represents either system, the only difference being the point which is considered to provide the output $C_1(z)$ or $C_2(z)$. As may be seen in the diagram, $C_1(z)$ may be examined by applying another sample-hold circuit, T-H-3, as shown while $C_2(z)$ is available as the output of T-H-2. Various methods may be used for calculating the output of such a system, of which the most straightforward is given by Kuo [5] and requires use of the "modified" z-transform, Z_m. Specifically, for this system

$$C_1(z) = \frac{H(z) \sum_{n=0}^{N-1} Z[\, e^{-nTs/N} \, G(s)\,]\ Z[\, e^{nTs/N} \, R(s)\,]}{1 + \sum_{n=0}^{N-1} Z[\, e^{-nTs/N} \, G(s)\,]\ Z[\, e^{nTs/N} \, H(s)\,]} \tag{22}$$
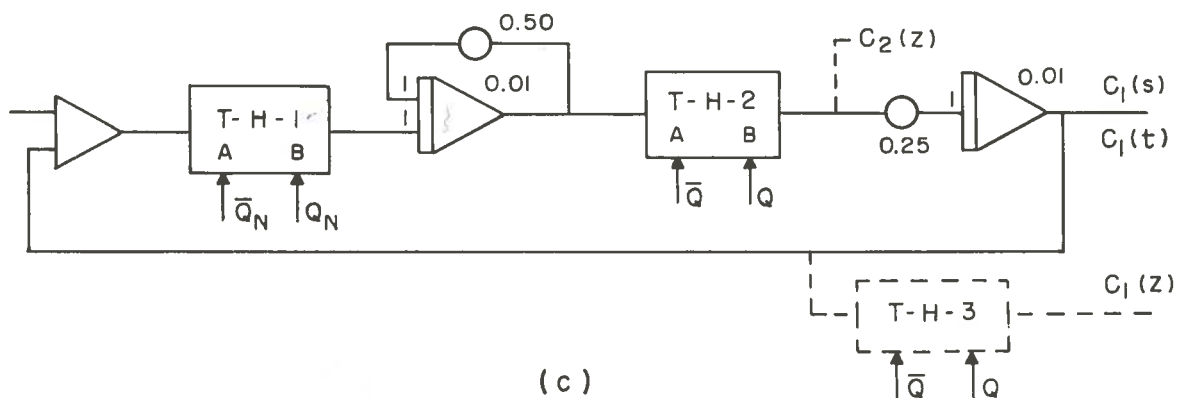
This has been worked out in Appendix D where calculations have been carried far enough to remove any possibility of undetected error. The photograph in Fig. 14 (d) shows the
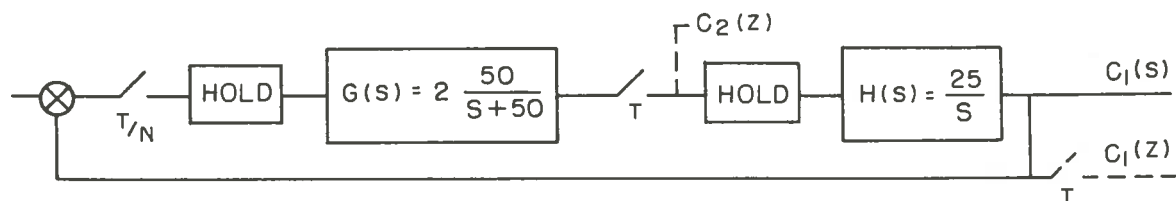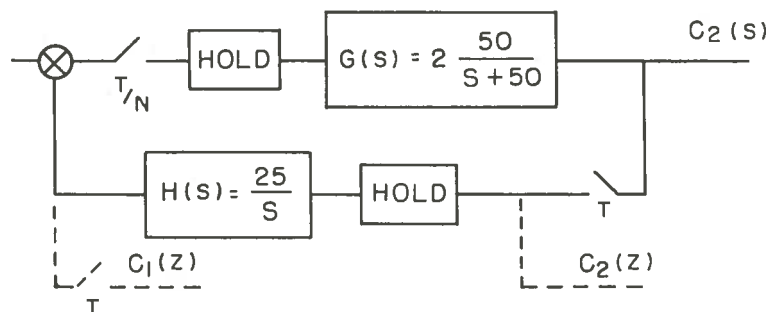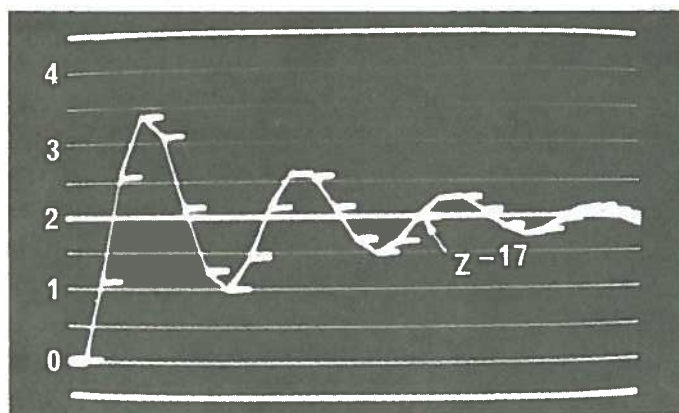
Figure 14 Two-plant system with two sampling rates
(a) Both plants in forward path; (b) One plant in feedback path;
(c) Simulation diagram; (d) $C_1(t)$ and $C_1(z)$ +HOLD outputs (no compensation).

$C_1(t)$ and $C_1(z)$ outputs with a sample-hold circuit applied to delineate the values at the sampling instants. These may be compared with calculated values which are as follows (see Appendix D) using an input step of 2 units

$$C_1(z) = 1.264\, z^{-2} + 2.744\, z^{-3} + 3.462\, z^{-4} + 3.114\, z^{-5}$$

$$+ 2.129\, z^{-6} + 1.255\, z^{-7} + \ldots + 1.969\, z^{-17} + \ldots \qquad (23)$$

Note the good agreement throughout the series up to z^{-17} which is within measurement error on the oscilloscope trace. As may be seen, the system, though not unstable, is quite oscillatory, and would benefit from some digital compensation. The exact procedure to use for this calculation is not immediately apparent but, on a trial basis, one may utilize some of the calculations already performed and demonstrate the particular usefulness of the simulation when used in conjunction with a minimum of calculation. It is convenient to lump the two plants together and use part of the denominator of equation (22)

$$G(z)\,H(z) = \sum_{n=0}^{N-1} Z\left[\,e^{-nTs/N}\,G(s)\,\right]\; Z\left[\,e^{nTs/N}\,H(s)\,\right]$$

$$= \frac{0.197\,(z + 2.21)}{(z - 1)\,(z - 0.368)} \qquad \text{(See Equation 6, Appendix D)}$$

Following the procedure as given in Appendix B, (substituting $G(z)\,H(z)$ for $G(z)$), it is found that suitable digital compensation would be

$$D(z) = \frac{2.35 - 0.77\,z^{-1}}{1 + 0.91\,z^{-1}} \qquad (24)$$

When this digital flow equation is simulated using the diagram of Fig. 7 (b) and connected in the system at the slow sampling switch, T, in Fig. 14 (a) the output response, $C_1(z)$, to a step is shown in curve A, Fig. 15 where the output is sampled as before to delineate the values.
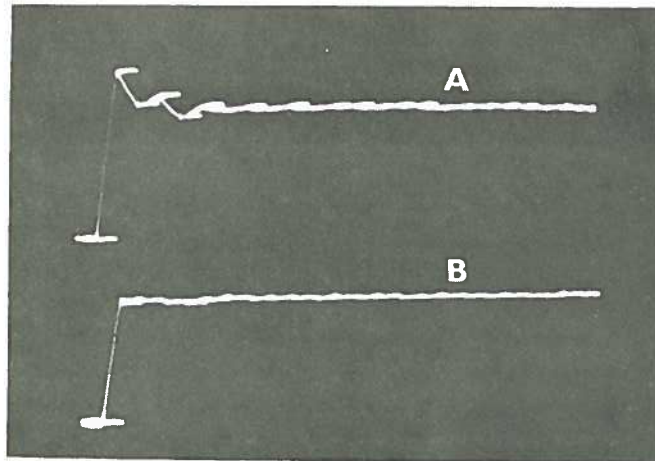

Figure 15 Step response of the two-plant, two-rate system
of Figure 14 using digital compensation.
Curve A - Response using calculated compensation
Curve B - Improved response found during simulation.

While this response may be acceptable, it is a simple matter to manipulate the coefficients of the simulated digital software, and discover the near dead-beat response shown in Curve B.. The new software constants can be read off the dials directly and in this case the dead-beat digital compensation is

$$D_1(z) = \frac{1.78 - 0.78\,z^{-1}}{1 + 0.70\,z^{-1}} \tag{25}$$

Conclusions

It will be evident that there are many advantages in simulating digital control systems in the manner described particularly when the effects of multi-rate sampling are to be investigated. The complexity of the mathematics for multi-rate systems for even the simple examples demonstrated is rather frightening and it is easy to predict that it becomes quite unmanageable as the number of rates and the order of the plants is increased. On the other hand, the analog computer with digital logic can easily simulate several sampling rates of any reasonable ratios while representing the plants in conventional fashion and can present a complete "live-model" system so helpful in obtaining an insight into dynamic characteristics. In many cases, a complete mathematical solution is no longer necessary, and excessive reliance on mathematical formulae which often mask real results is reduced.

One other aspect which is worth mentioning is the educational potential of the technique particularly when used with a multi-beam oscilloscope as was done in the current study. For greatest benefit, the student should have some prior acquaintance with digital computers and their associated equipment, and with z-transforms. With this equipment, fundamental concepts of sampling, holding, partial and interval delays, acquisition time, compute time, overloading, etc., can be demonstrated and are more readily understood because they can be "seen" and manipulated. Then, as the student progresses to setting up and solving problems, the almost direct correspondence of the mathematics and the hardware is particularly advantageous in the learning process.

References

1. R. Saucedo and T.W. Sze, "Analog Simulation of Digital Computer Programs", AIEE Trans. Communications and Electronics, Jan. 1962.

2. Y.J. Kingma, "Analog Simulator for Digital Controllers", Simulation Vol. 10, No. 2, Feb. 1968.

3. J.R. Ragazzini and G.F. Franklin, "Sampled-Data Control Systems", McGraw-Hill Book Co., 1958.

4. Eliahu I. Jury, "Sampled-Data Control Systems", John Wiley & Sons Inc., 1958.

5. Benjamin C. Kuo, "Analysis and Synthesis of Sampled-Data Control Systems", Prentice-Hall Inc., 1963.

APPENDIX A

Calculation of Output of a Closed-Loop Digital System

From equation (11) of text

$$C(z) = \frac{K\,G_{ho}\,G_1\,(z)}{1 + K\,G_{ho}\,G_1(z)}\;R(z)\quad.$$

Then, using equation (10) of text, and a unit step input,

$$C(z) = \frac{\dfrac{0.424\,z^{-1} + 0.364\,z^{-2}}{(1 - z^{-1})\,(1 - 0.606\,z^{-1})}}{1 + \dfrac{0.424\,z^{-1} + 0.364\,z^{-2}}{(1 - z^{-1})\,(1 - 0.606\,z^{-1})}}\;\times\;\frac{1}{1 - z^{-1}}$$

$$= \frac{0.424\,z^{-1} + 0.364\,z^{-2}}{1 - 1.182\,z^{-1} + 0.970\,z^{-2}}\;\times\;\frac{1}{1 - z^{-1}}$$

Simplifying by long division

$$C(z) = 0.42\,z^{-1} + 1.29\,z^{-2} + 1.90\,z^{-3} + 1.78\,z^{-4} + 1.07\,z^{-5} + \ldots.$$

APPENDIX B

Ripple-Free Design of a Single-Rate System

To design a ripple-free system which will achieve steady-state in a minimum number of sampling intervals, sampled-data theory requires that:

$$D(z) = \frac{K(z)}{1 - K(z)} \cdot \frac{1}{G(z)} \tag{1}$$

and that $K(z)$ should contain all the zeros, z_i, of $G(z)$, and be of the form:

$$K(z) = (1 - z_i z^{-1})(a_0 + a_1 z^{-1} + \cdots)$$

and that $1 - K(z)$ should contain all the poles, p_i, of $G(z)$, plus a factor $(1 - z^{-1})^n$, where $n = 2$ for an input ramp signal, and be of the form

$$1 - K(z) = (1 - p_i z^{-1})(1 - z^{-1})^n (1 + b_1 z^{-1} + \cdots)$$

In this case, for the plant transfer function,

$$G(z) = \frac{0.424 z^{-1} (1 + 0.860 z^{-1})}{(1 - z^{-1})(1 - 0.606 z^{-1})} \tag{2}$$

and an input ramp, a digital compensation network suitable for illustrating a simulation will be derived by taking

$$K(z) = z^{-1} (1 + 0.860 z^{-1})(a_0 + a_1 z^{-1})$$

and

$$1 - K(z) = (1 - z^{-1})^2 (1 + b_1 z^{-1})$$

in which the values of a_0, a_1 and b_1 are found by equating coefficients of like powers of z to obtain

$$a_0 = 1.324$$
$$a_1 = -0.786$$
$$b_1 = 0.676$$

whence

$$K(z) = z^{-1} (1 + 0.860 z^{-1})(1.324 - 0.786 z^{-1})$$
$$= 1.324 z^{-1} + 0.353 z^{-2} - 0.674 z^{-3} \tag{3}$$

and

$$1 - K(z) = (1 - z^{-1})^2 (1 + 0.676 z^{-1}) \tag{4}$$

then

$$D(z) = \frac{Kz}{1 - K(z)} \quad \frac{1}{G(z)}$$

$$= \left[\frac{z^{-1}(1 + 0.860 \, z^{-1})(1.324 - 0.786 \, z^{-1})}{(1 - z^{-1})^2 \, (1 + 0.676 \, z^{-1})} \right] \times \left[\frac{(1 - z^{-1})(1 - 0.606 \, z^{-1})}{0.424 \, z^{-1} \, (1 + 0.860 \, z^{-1})} \right]$$

$$(5)$$

$$= \frac{3.123 - 3.745 \, z^{-1} + 1.123 \, z^{-2}}{1 - 0.324 \, z^{-1} - 0.676 \, z^{-2}}$$

Compensation Design for a Multi-Rate System

For a multi-rate system such as shown in Fig. 13(a), and an input signal of $R(s) = \dfrac{1}{s^k}$ a suitable system transfer function has the form:

$$K(z_n) = \frac{(1 - z_n^{-n})^k}{(1 - z_n^{-1})^k} \; (a_0 z_n^{-1} + a_1 z_n^{-2} + \cdots) \tag{1}$$

When the input is a ramp, $R(s) = \dfrac{1}{s^2}$ and equation (1) becomes

$$K(z_n) = \left[\frac{1 - z_n^{-n}}{1 - z_n^{-1}} \right]^2 \; \left(\frac{n+1}{n} \; z_n^{-1} - z_n^{-2} \right) \tag{2}$$

Further, it can be shown that the compensation network

$$D(z_n) = \frac{1}{G(z_n)} \; \frac{K(z_n)}{1 - K(z_n^{\,n})} \tag{3}$$

and

$$K(z_n^{\,n}) = 2 z_n^{-n} - z_n^{-2n}$$

so that

$$1 - K(z_n^{\,n}) = 1 - 2 z_n^{-n} + z_n^{-2n}$$

$$= (1 - z_n^{-n})^2 \tag{4}$$

Let the z_n-transform of the hold circuit and the plant be

$$G(z_n) = Z\left[\frac{1 - e^{-sT/n}}{s} \right] \left[\frac{a}{s+a} \right] = \frac{(1 - z_n^{-1})(1 - e^{-aT/n})z_n^{-1}}{(1 - z_n^{-1})(1 - e^{-aT/n} z_n^{-1})}$$

$$= \frac{(1 - e^{-aT/n}) z_n^{-1}}{1 - e^{-aT/n} z_n^{-1}} \tag{5}$$

Then, substituting (5), (2) and (4) in (3) the digital controller is found to be:

$$D(z_n) = \frac{1 - e^{-aT/n} z_n^{-1}}{(1 - e^{-aT/n}) z_n^{-1}} \times \frac{\left[\dfrac{1 - z_n^{-n}}{1 - z_n^{-1}} \right]^2 \left[\dfrac{n+1}{n} z_n^{-1} - z_n^{-2} \right]}{(1 - z_n^{-n})^2}$$

$$= \frac{(1 - e^{-aT/n} z_n^{-1}) \left[\dfrac{n+1}{n} - z_n^{-1} \right]}{(1 - e^{-aT/n}) (1 - z_n^{-1})^2}$$

Taking $a = 6.90$, $T = 1.0$ sec. (selected for convenience)

$$D(z_1) = \frac{1 - 0.001\, z_1^{-1}}{0.999} \times \frac{2.00 - z_1^{-1}}{(1 - z_1^{-1})^2} = \frac{2.001 - 1.003\, z_1^{-1} + 0.001\, z_1^{-2}}{1 - 2\, z_1^{-1} + z_1^{-2}}$$

$$D(z_2) = \frac{1 - 0.032\, z_2^{-1}}{0.968} \times \frac{1.50 - z_2^{-1}}{(1 - z_2^{-1})^2} = \frac{1.55 - 1.080\, z_2^{-1} + 0.033\, z_2^{-2}}{1 - 2\, z_2^{-1} + z_2^{-2}}$$

$$D(z_4) = \frac{1 - 0.178\, z_4^{-1}}{0.820} \times \frac{1.25 - z_4^{-1}}{(1 - z_4^{-1})^2} = \frac{1.52 - 1.49\, z_4^{-1} + 0.219\, z_4^{-2}}{1 - 2\, z_4^{-1} + z_4^{-2}}$$

APPENDIX D

Calculation of Output for a Two-Plant, Two-Rate System

For the system shown in Fig. 14(a) with $N = 2$, $T = 0.02$

$$C_1(z) = \frac{H(z) \sum_{n=0}^{N-1} Z\left[e^{-nTs/N} G(s)\right] Z\left[e^{nTs/N} R(s)\right]}{1 + \sum_{n=0}^{N-1} Z\left[e^{-nTs/N} G(s)\right] Z\left[e^{nTs/N} H(s)\right]} \tag{1}$$

where $G(s)$ and $H(s)$ include their respective HOLD circuits.

$$Z\left[e^{-nTs/N} G(s)\right] = Z\left[e^{-nTs/2} \frac{(1-e^{-Ts/2})100}{s(s+50)}\right]$$

$$= Z_m\left[\frac{100}{s(s+50)}\right]_{m=\frac{n}{2}} - Z_m\left[\frac{100}{s(s+50)}\right]_{m=1-\frac{n+1}{2}}$$

for $n = 0$
$$= 2\left[\frac{1}{z-1} - \frac{e^{-1}}{z-e^{-1}}\right] - 2\left[\frac{1}{z-1} - \frac{e^{-0.5}}{z-e^{-1}}\right] = \frac{0.476}{z-0.368} \tag{2}$$

for $n = 1$
$$= 2\left[\frac{1}{z-1} - \frac{e^{-0.5}}{z-e^{-1}}\right] - 2\left[\frac{1}{z-1} - \frac{e^{0}}{z-e^{-1}}\right] = \frac{0.788}{z-0.368}$$

and
$$Z\left[e^{nTs/N} H(s)\right] = z Z_m\left[\frac{25(1-e^{-sT})}{s^2}\right]_{m=\frac{n}{2}} = (z-1) Z_m\left[\frac{25}{s^2}\right]_{m=\frac{n}{2}}$$

for $n = 0$
$$= (z-1) \frac{0.5}{(z-1)^2} = \frac{0.5}{z-1}$$

for $n = 1$
$$= (z-1) \frac{0.25(z-1) + 0.5}{(z-1)^2} = \frac{0.25(z+1)}{z-1} \tag{3}$$

and
$$Z\left[e^{nTs/N} R(s)\right] = z Z_m\left[\frac{2}{s}\right]_{m=\frac{n}{2}} = \frac{2z}{z-1} \quad \text{for } n = 0 \text{ and } n = 1 \tag{4}$$

and
$$Z\left[H(s)\right] = Z\left[\frac{25(1-e^{-sT})}{s^2}\right] = \frac{0.5}{z-1} \tag{5}$$

Substituting equations (2), (3), (4) and (5) in (1),

$$C_1(z) = \cfrac{\dfrac{0.5}{z-1}\left[\dfrac{0.476}{z-0.368}\times\dfrac{2z}{z-1}+\dfrac{0.788}{z-0.368}\times\dfrac{2z}{z-1}\right]}{1+\left[\dfrac{0.476}{z-0.368}\times\dfrac{0.5}{z-1}+\dfrac{0.788}{z-0.368}\times\dfrac{0.25\,(z+1)}{z-1}\right]}$$

$$= \cfrac{\dfrac{1.264\,z}{(z-1)^2\,(z-0.368)}}{1+\dfrac{0.197\,(z+2.21)}{(z-1)\,(z-0.368)}} \tag{6}$$

$$= \frac{1.264\,z}{z^3 - 2.171\,z^2 + 1.974\,z - 0.803} \tag{7}$$

$$= 1.264\,z^{-2} + 2.744\,z^{-3} + 3.462\,z^{-4} + 3.114\,z^{-5}$$

$$+ 2.129\,z^{-6} + 1.255\,z^{-7} + 1.022\,z^{-8} + 1.451\,z^{-9}$$

$$+ 2.141\,z^{-10} + 2.605\,z^{-11} + 2.594\,z^{-12} + 2.209\,z^{-13}$$

$$+ 1.768\,z^{-14} + 1.560\,z^{-15} + 1.671\,z^{-16} + 1.969\,z^{-17} + \cdots$$