Supplementary material

Gate controlled quantum dots in monolayer WSe2

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1. Device Fabrication and AFM Cleaning

The fabrication process uses a dry transfer technique based on subsequent “pick-up” and “drop-off” of flakes of 2D materials on top of one another.

The transfers are done with a polypropylene carbonate (PPC) / polydimethylsiloxane (PDMS) stamp as support for the flakes. The PDMS in these stamps is treated with an oxygen plasma before being covered with PPC. This ensures that the PPC will remain adhered to the PDMS during the transfer. For hBN, using this PPC/PDMS stamps, flakes can be picked up at a temperature of ≈ 40°C and dropped off at a temperature of ≈ 70°C. The PPC/PDMS stamp is used to pick-up an exfoliated hBN flake which is dropped off onto the local control gates. After depositing and cleaning the contacts (Cr (2nm) / Pt (8 nm))[1], a PPC/PDMS stamp is used to pick-up another exfoliated hBN flake. The hBN on the stamp is used to pick-up an additional flake of WSe2. This stack of hBN/ WSe_2 flake is then deposited on top of the contacts. Finally, the top gate is patterned.

We use an AFM tip to mechanically clean the 2D material[2,3] and the contacts[4] immediately before the deposition of the WSe_2/hBN stack.

Figure S1 demonstrates the effects of such a mechanical cleaning technique where an AFM topographic map of the sample after AFM cleaning is shown (Figure S1(a)). The bright rectangle surrounding the area that was cleaned represents the accumulation of residues at the perimeter of the scanning area. Figure S1(b) shows a line profile across the contaminant boundary (indicated by the dashed arrow in Figure S1(a)) in which we indicate the cleaned area, the residues and the area that was not cleaned.

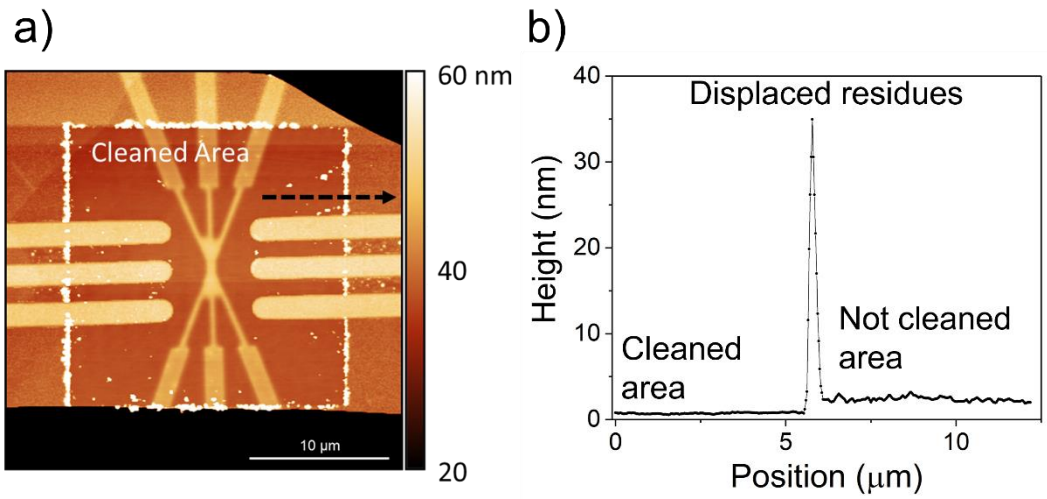
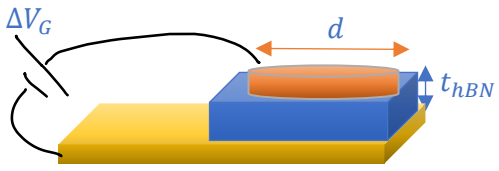


Figure Supplementary 1. (a) Atomic force microscopy (AFM) topographic map of the device immediately after AFM cleaning where the residues are visibly swept to the perimeter of the cleaning area. (b) A line profile corresponding to the black dashed arrow in (a) taken across the contaminant boundary.

2. Quantum dot size estimation

The model we used to estimate the dot size of the quantum dot is schematically represented below.



Based on the planar geometry of the device, we use a parallel plate capacitor model where one plate is the local control gate and the other is the quantum dot itself, separated by the thickness t_{hBN} of the hBN dielectric. When a voltage ΔV_G is applied between the gate and the dot, one can estimate a dot diameter d as shown below:

$$Capacitance = \frac{e}{\Delta V_G} = \frac{\epsilon_0 \epsilon_{hBN}\, Area\ of\ the\ dot}{t_{hBN}} => d = \sqrt{\frac{4 t_{hBN} e}{\epsilon_0 \epsilon_{hBN} \pi \Delta V_G}}$$

We note that there is some uncertainty in the estimated size of the dot that can come from the value used for the dielectric constant of hBN. We use $\epsilon_{hBN} = 4$ to obtain the value in the main text, however there are multiple values quoted in literature. Table S1 summarizes some of the possible values for ϵ_{hBN} and the associated quantum dot size d.

Table S1

ϵ_{hBN}	Reference	d (nm)
3 – 4	Ref. 5	58 - 67
2.5 – 3.5	Ref. 6	62 - 73
3.5 – 3.8	Ref. 7	60 - 62
2 – 4	Ref. 8	58 - 82

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