Six-decade counter for luminescence spectra
O'Hara, D. H.; McDougall, J.

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SIX - DECADE COUNTER FOR LUMINESCENCE SPECTRA

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ABSTRACT

A six-decade up-down counter is described in
detail.   The instrument has been interfaced with
an existing data recording system for lumines-
cence spectra. The sample period is selectable
in two ranges from 1 msec to 100 seconds.

CONTENTS

FIGURES

PLATES

SIX-DECADE COUNTER FOR LUMINESCENCE SPECTRA

- D.H. O'Hara and J. McDougall -

A system for automatic data recording for luminescence spectra measurements was described in an earlier report [1]. Two variables, wavelength and luminescence intensity, are measured, digitized, and arranged in a format for direct entry into a computer on a magnetic tape recording. Wavelength, as represented by the shaft angle of a monochromator, is the independent variable and readings are initiated by the monochromator drive at adjustable intervals of wavelength. The output current of a photomultiplier tube is a measure of the luminescence intensity.

At high luminescence intensities the integrated current output of the photomultiplier tube is a convenient data form. The original system described in ERB-746 was designed to digitize this analog signal for recording. At low luminescence intensities photon counting techniques are desirable. The output of the photomultiplier consists of discrete pulses which, after amplification and pulse height discrimination need only be counted to provide a digital representation of luminescence intensity. The counter described in this report now extends the system capability to discrete signal inputs. Figure 1 is a block diagram of the expanded system when used for pulse counting.
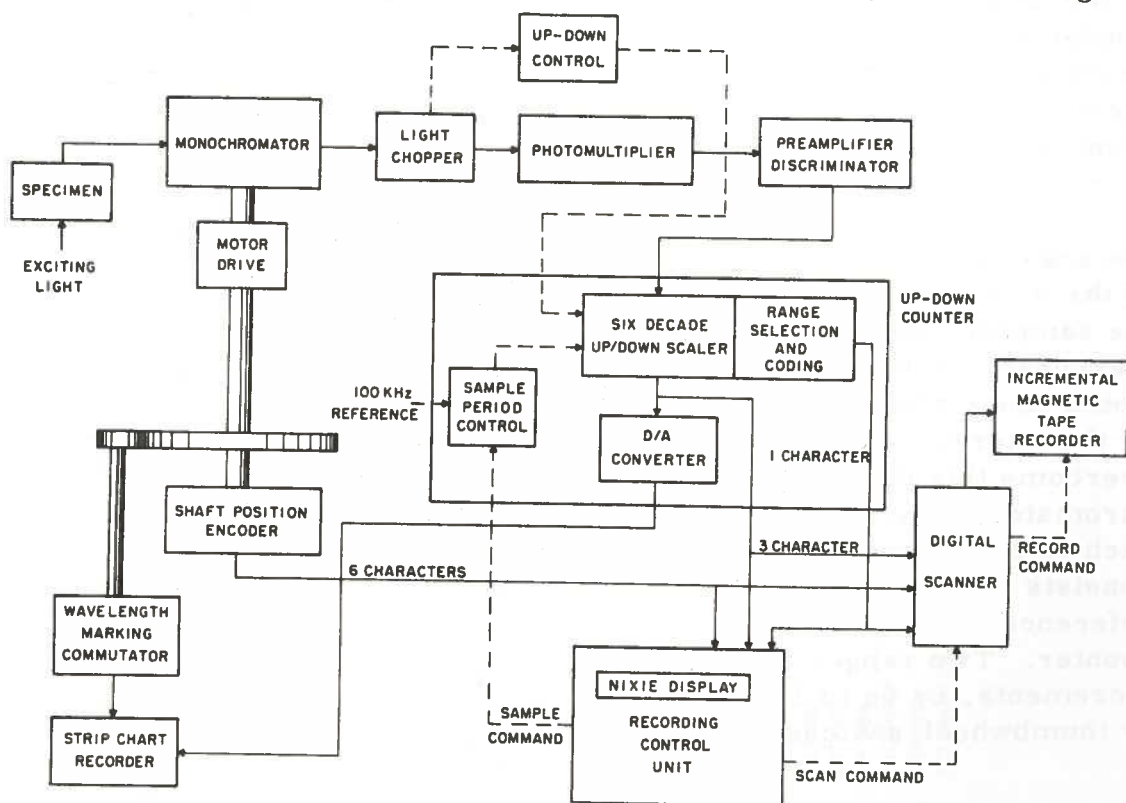

Figure 1 Data recording system block diagram

The basic unit is a six-decade up-down synchronous counter with buffered readout for three digits only. Range is manually selected in decade steps by a front-panel switch. A one-digit readout for the exponent is coded by this switch. Sampling period is selectable from 1 msec to 100 seconds. Analog display of the count in the buffer is also provided. Resistor-transistor-logic integrated circuits have been used for all counting functions. Figure 2 is a block diagram of the counter, and Plate I shows the front panel layout of the counter.

A bi-directional counter was used in an attempt to remove some of the noise added by the measuring instruments. This is done by using a mechanical chopper to interrupt periodically the luminescence light and subtract the count generated by the photomultiplier tube in the dark period from the previously accumulated total. The counting mode may be electrically controlled or it may be set to count "up" by a front-panel switch. The counter is designed to insure that pulses are not lost during the change in counting direction. Counting rate is 900 kHz in the bi-directional mode or 2.5 MHz in the count-up mode.

Data recorded on magnetic tape cannot be edited, conveniently, before computer processing. The experimenter will have greater confidence in his measurement if he is presented with a display of his data at the time they are being recorded. For this purpose a digital-to-analog converter which changes 2 digits (1% resolution) of the accumulated count to an analog voltage for display on a strip-chart recorder was included. Full scale display of 1000 or 100 counts is selected by a front-panel switch.

Although time is not an explicit variable in the measurement, the angular rotation rate of the monochromator shaft and the resolution of the measurement (wavelength intervals between samples) determine the sampling period. Variation in monochromator drive speed and inaccuracy in the shaft angle digitizer (an absolute shaft position encoder) would cause a non-constant sampling period if the period was controlled by the interval between equal indicated increments of wavelength. To overcome this difficulty, an adjustable clock is included. The monochromator drive still determines the sampling rate but the duration of each sampling period is accurately timed by the clock. The clock consists of a pre-settable four-decade down counter. A 100-kHz reference signal, divided to either 1000 Hz or 100 Hz, drives the down counter. Two ranges of sample period, up to 10 seconds in 1 msec increments, or up to 100 seconds in 10 msec increments, may be selected by thumbwheel switches.
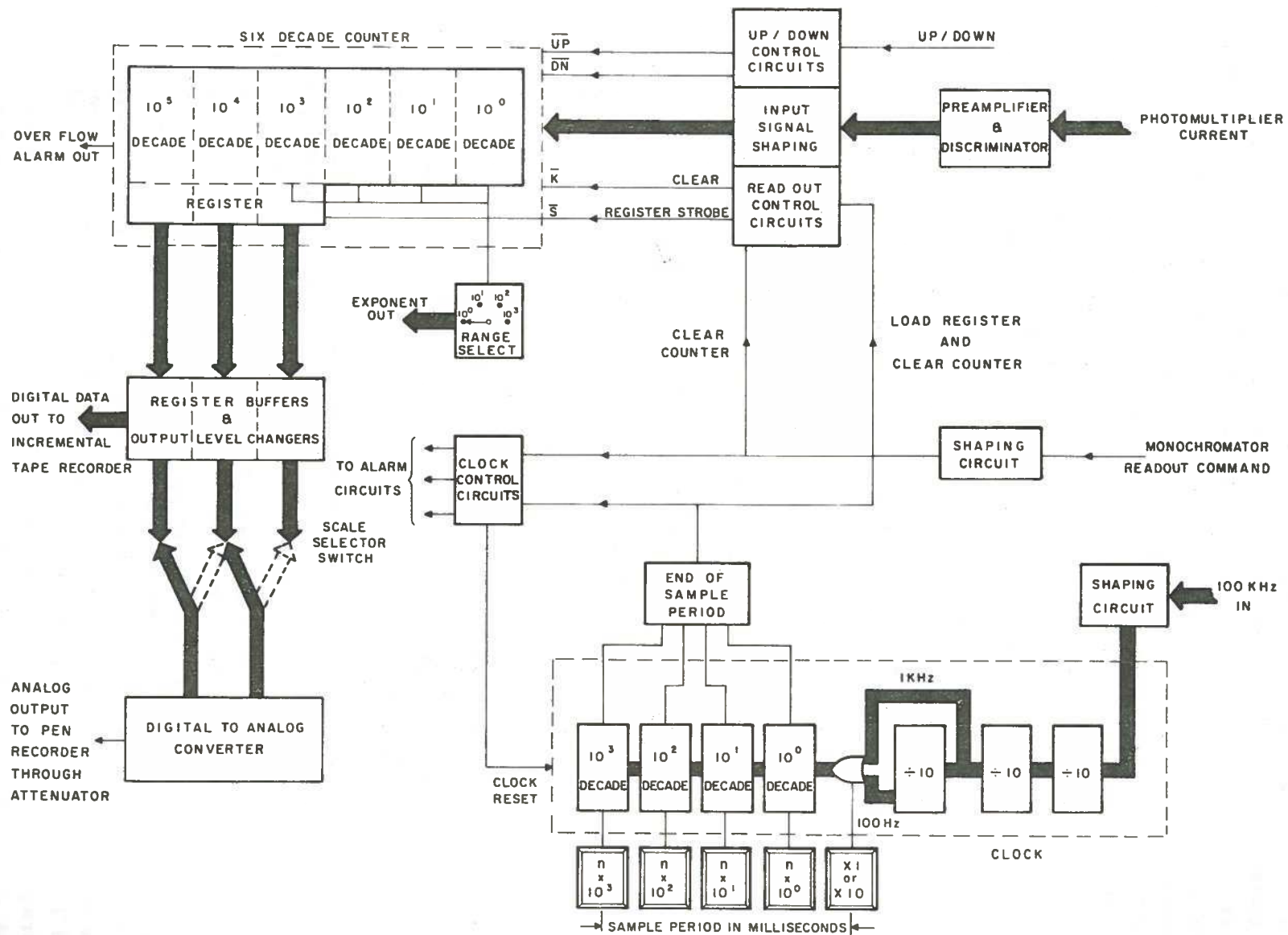
Figure 2 Counter block diagram

An audio-visual alarm indicates three undesirable conditions; (a) counter overflow, (b) sample period too long, (c) sample period too short. Conditions (a) and (b) will cause incorrect data to be recorded. Condition (c) means a loss in signal-to-noise ratio, since the full interval which is available to count pulses is not being used. The alarm for counter overflow must be manually reset, but the other two conditions trigger momentary alarm indications only.
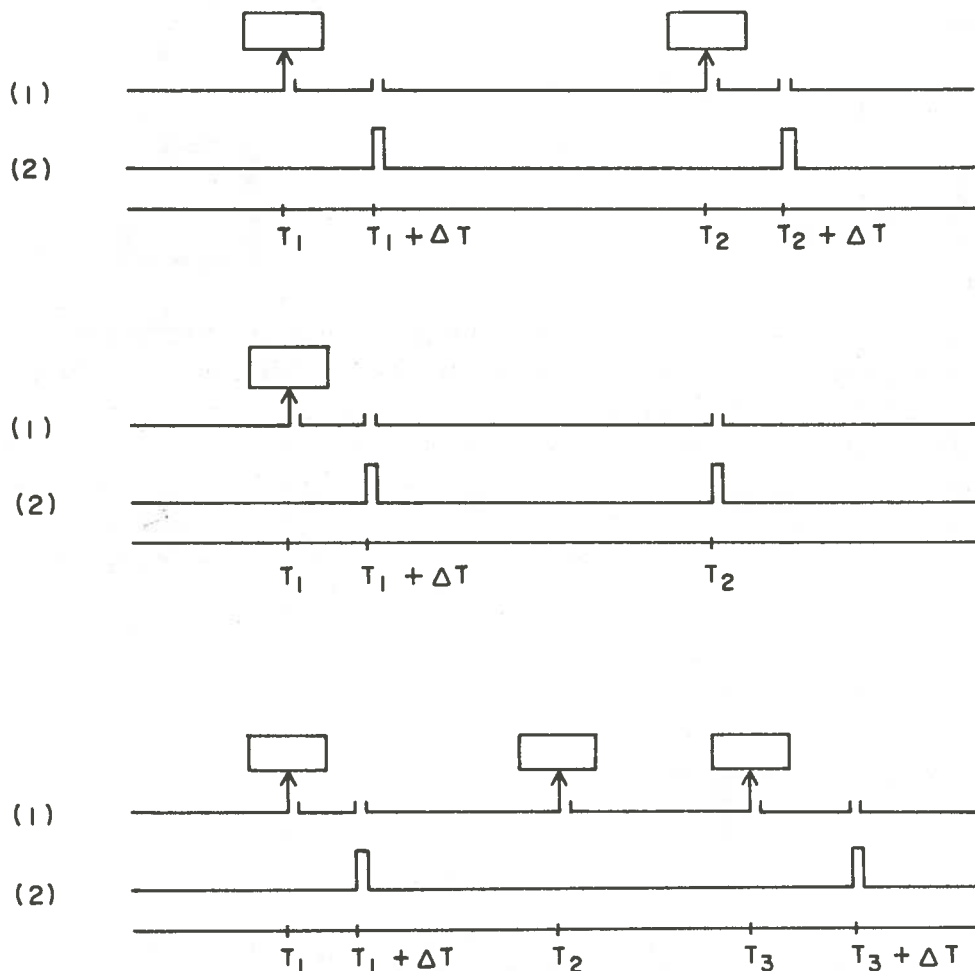
(1) Clock Initiated Data Transfer to Storage Register.
(2) Monochromator readout command.

Figure 3 Counter readout sequence; a) normal sequence, b) sample period too long, c) sample period too short

Figure 3 is a timing diagram showing sampling sequences. The sequence shown in Fig. 3(a) is considered normal. At times T_1 and T_2 the clock initiates the data transfer from the counter to the storage register, clears the counter and recycles itself. At times $T_1 + \Delta T$ and $T_2 + \Delta T$ a readout command from the monochromator

drive starts the recording process. This pulse also clears the counter and resets the clock. Data in the storage register are unchanged. The normal recording mode then has the interval between monochromator readout commands almost equal to the clock period, but always slightly longer. Dead-time is then ΔT.

The "sample period too long" alarm condition is shown in Fig. 3 (b). Here the monochromator readout command has occurred at T_2 before the clock was able to transfer the new count to the storage register. Therefore, data recorded at T_2 will be same as recorded at $T_1 + \Delta T$. As long as the clock sample period remains longer than the time between monochromator generated readouts, incorrect data will be recorded.

The condition indicated by the "sample period too short" alarm exists in Fig. 3 (c). In this instance a second data transfer from the counter to the storage register will have been initiated by the clock without the first sample having been recorded. Although the count recorded at T_2 is valid, less than half the time available to accumulate counts has been used.

CIRCUIT DETAILS

The counter is separated into three sections for detailed description. These are (a) the six decade up/down counter, (b) the clock section which sets the sample length, and (c) the interface for the output and for the digital-to-analog converter. The standard symbols used in the logic diagrams are shown in Fig. 1 of the Appendix. Detailed wiring diagrams for the counter are listed in the appendix also.

Six Decade Up/Down Counter

The counter is a synchronous BCD (8421) up/down counter. Each decade requires one printed circuit board. All six are similar, with minor differences for carry control wiring and only the upper three decades have storage registers. Each decade must decode the carry control lines from all the lower decades. Range control is achieved by overriding the carry control gating to by-pass lower decades as the range is decreased. For example, for a full scale range of 999×10^1 the carry control to the 10^2 decade is permanently enabled by the range switch so that input pulses are gated to the 10^2 decade. The Boolean expression for carry control is

$$C = UP.9 + DOWN.0 + R$$

where R is range control and is present on the three lower decades only. Figure 4 is the schematic of the 10^3 decade.
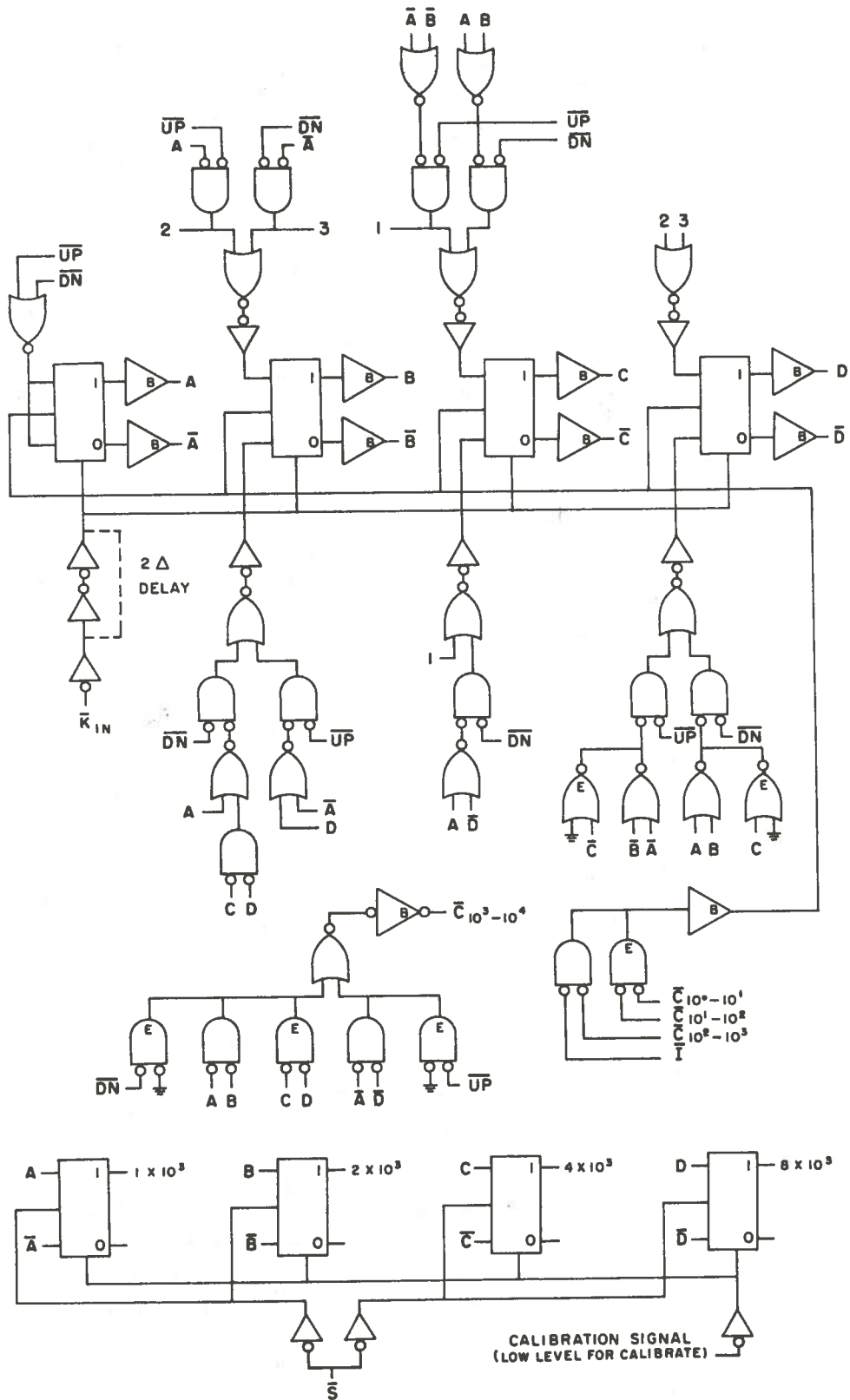
Figure 4 10^3 decade of the six decade UP-DOWN counter

Three external inputs affect the counter (a) pulse to be counted, (b) counting mode control, i.e., up or down, (c) readout command. After a change in each of these inputs a period exists in which the counter reaction to further changes is unpredictable. Therefore, a command to change counting mode or read out accumulated count is delayed long enough for a transient due to a count pulse to decay. Similarly, count pulses are inhibited during a change in count mode or during readout. However, a pulse occurring during a change in counting mode is added when the counter is stable again. A count pulse occurring during read-out is ignored. The counter is vulnerable at excessive count pulse rates. This is not a problem now as the discriminator limits the pulse rate to a value well below the critical rate. The critical rate will be discussed after the input control circuitry has been described.

The three one-shot multivibrators I_0, I_1, and $\overline{I}$ in Fig. 5, which have a period of nominally 100 nsec, condition the output of the discriminator pulses. The $\overline{I}$ one-shot multivibrator triggers the counter. The signal inputs from B, C, X, I_0, and $\overline{I}_{INHIBIT}$ to the gate circuits between I_1 and $\overline{I}$ inhibit counting during transient instabilities of the counter. The L signal is raised if a count pulse occurs during a change in count mode. When the inhibits are removed the presence of the L signal will trigger I and add a count.

The direction of counting, i.e., up or down, is controlled by a square wave signal labeled A in Fig. 5. A positive transition sets the counter to count down. The timing sequence for change in counting direction from up to down is shown in Fig. 6. A low level (ground potential) signal on $\overline{DN}$ forces the counter to count down. The positive transition of A at T_1 generates the B signal which stops further counting by inhibiting the I_1 signal. A change in up-down control signal occurring at T_2 will not reach the counter before all changes of state due to a count pulse which must have occurred prior to T_1 have been completed. At T_2 the D signal goes down and generates the E signal which enables B to set the up-down latch circuit to down. The B signal persists until T_3, by which time the counter is again ready to count. The sequence for readout is similar. The X signal corresponds to B and the $\propto$ signal going down generates the register strobe signal, $\overline{S}$. The counter clear signal $\overline{K}$ is generated by the S signal as it goes down. The time delays are shown on the one-shot multivibrators in Fig. 5.
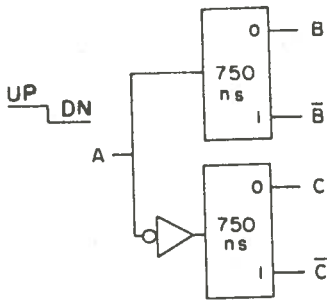
UP-DOWN SEQUENCE CONTROL
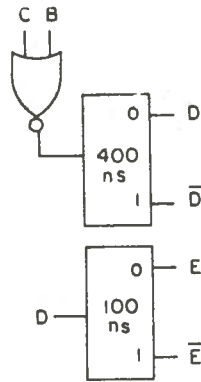
UP-DOWN LATCH
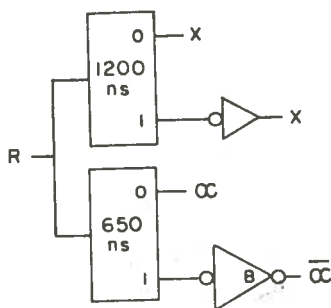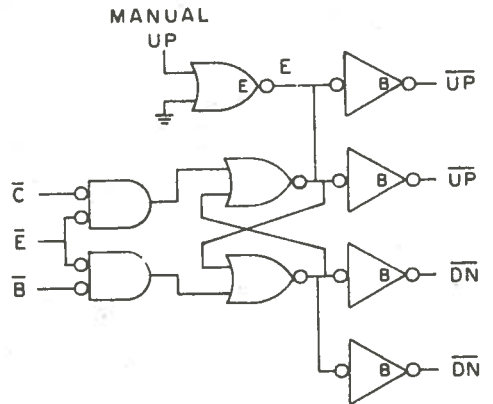
DATA TRANSFER CONTROL
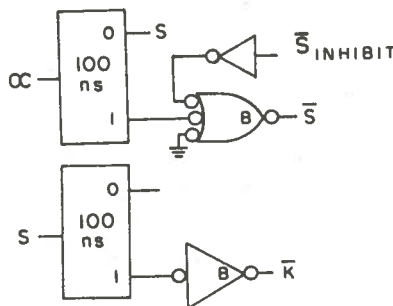
COUNTER INHIBIT FOR MODE CHANGES
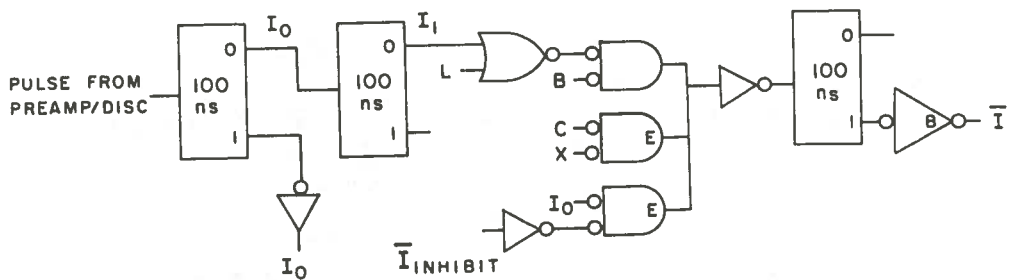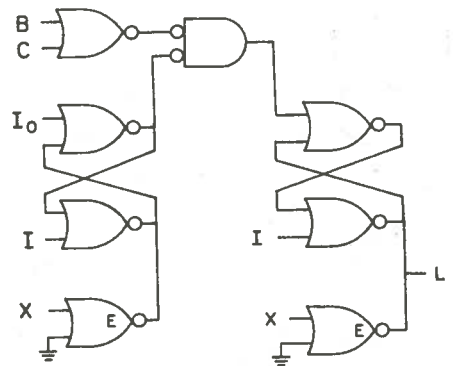
PULSE CONDITIONING

Figure 5   UP-DOWN counter input control circuits

As indicated earlier, no count pulses are lost during a change in count mode. This is accomplished by detecting coincidence between I_0 and B or C signals in the "coincidence latch" circuit in Fig. 5. The output of the latch circuit, L, triggers the counter when the change of counting mode inhibit (B or C) is removed. The count pulse input from the discriminator triggers the I_0 one-shot multivibrator.
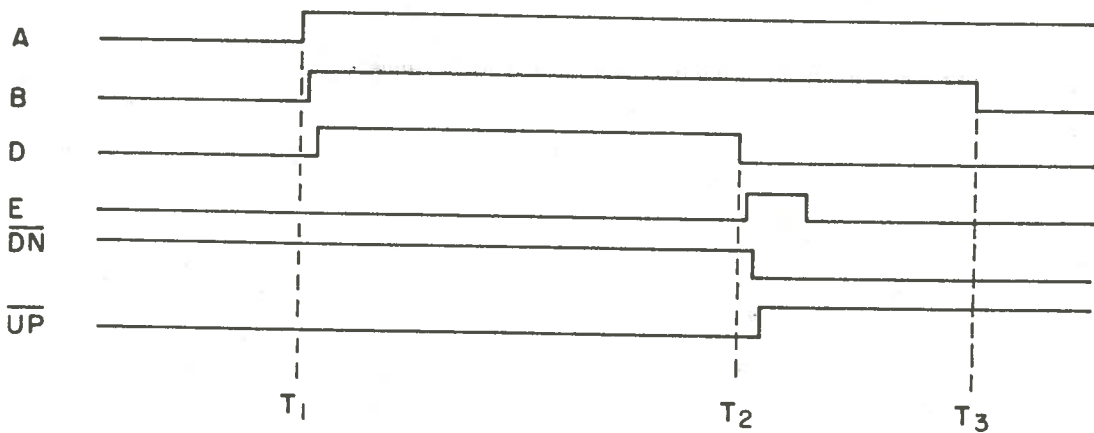
Figure 6 Timing sequence, change in counting direction from UP to DOWN

The trailing edge of I_0 triggers I_1 but the leading edge of I_1, delayed by three gate delays, triggers I. The I signal resets the "coincidence latch". By detecting coincidence between B or C signals and I_0 instead of I_1 the relative periods of I_1 and I one-shot multivibrators are made non-critical. If I_1 were used instead of I_0 the period of I_1 could increase, relative to the period of I, to the extent that the I signal would go down before I_1 and the coincidence latch would not be reset. The X signal resets the coincidence latch also, to avoid adding a pulse if readout command, change in count mode command, and a count pulse occur together. The I_0 signal input to the "coincidence latch" is taken from the output of a latch circuit in order to bridge what would otherwise be a "dead" period of one flip-flop delay and a gate delay in which B or C could inhibit pulse counting after I_0 one-shot signal had gone down. The I_0 signal must inhibit the I_1 signal to avoid double triggering if I_0 occurs just at the end of the B or C inhibit. The I one-shot would be triggered at times T_1 and T_2 in Fig. 7 if I_0 did not inhibit counting at T_1. The counter would react unpredictably to two pulses so close together. The inhibit signals $\overline{I}_{INHIBIT}$ and $\overline{S}_{INHIBIT}$ will be discussed in the section describing the clock.
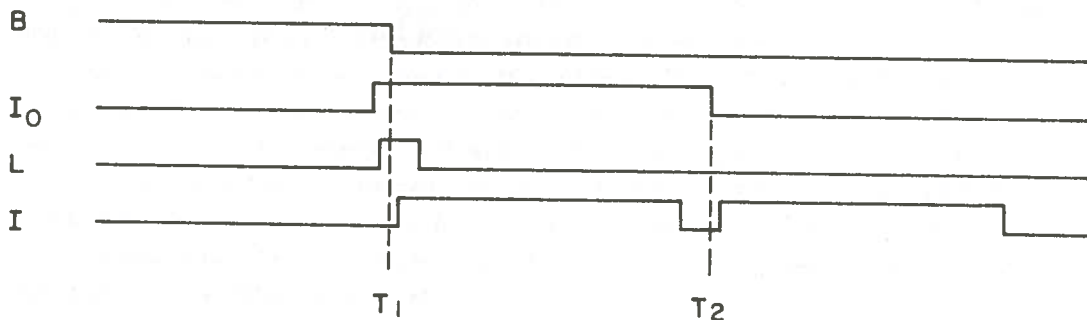

Figure 7 Timing sequence: reason for $I_{0\,INHIBIT}$ on I

To insure reliable operation the minimum pulse width is set at 100 nsec. The one-shot multivibrator delays, to allow counter settling, were calculated using the limits of the manufacturer's specified delays for the circuit elements. Using these figures, the counter should respond reliably to two 100-nsec pulses approximately 360 nsec apart or at pulse rate of 2.5 MHz. The counter has been tested up to 2.8 MHz. The B or C inhibits set up during a change in count mode last for 750 nsec. If a pulse occurs while they are raised, it is added immediately after, thus the total period between pulses to ensure that the counter is not upset by too closely spaced pulses must be greater than 1100 nsec (B or C, 750 nsec + pulse transient, 360 nsec). The maximum pulse rate for up-down counting is therefore $\simeq 900$ kHz.

The 999999 to 000000 transition triggers the counter over-flow alarm. However, the overflow detection circuit first must be enabled by a 5 count on the 10^5 decade. The 5 count sets a latch circuit which is reset each time the counter information is recorded by the register strobe. By using the "5 latch" to enable the overflow detect circuit, a false overflow alarm is avoided when the count down control occurs first in an up-down counting sequence. Under this condition a 000000, 999999. . . . 999999, 000000 sequence occurs but the counter has not overflowed.

Clock System

The clock consists of a 4-decade BCD (8421) synchronous down counter which may be preset. The pulse input to the counter is derived from an external 100-kHz reference divided to either 1000 Hz or 100 Hz. Each decade is preset by a BCD coded thumbwheel switch. A fifth thumbwheel switch selects either the 1000-Hz or 100-Hz driving signal. Counter information is transferred to the register when the clock down counter reaches a zero count. The preset input from the thumbwheel switches is then loaded into the clock down counter and the cycle begins again. However, the monochromator drive may at any instant re-initialize the clock down counter. Therefore, both "zero" as well as "one" states must be forced into the down counter. Since the J-K flip-flops used have only one DC control input, an expander circuit element was connected to the "one" output of the flip-flop to provide a "direct clear" DC control input. The output signal labeled $\overline{C}_{10}$ n$_{-10}$ n+1 is the decoded zero count of each decade. This signal is the carry control signal to the adjacent decade and is ANDed to provide a zero detect for the readout command generation. The logic circuitry for the down counter is shown in Fig. 8. Each printed circuit board holds two decades.
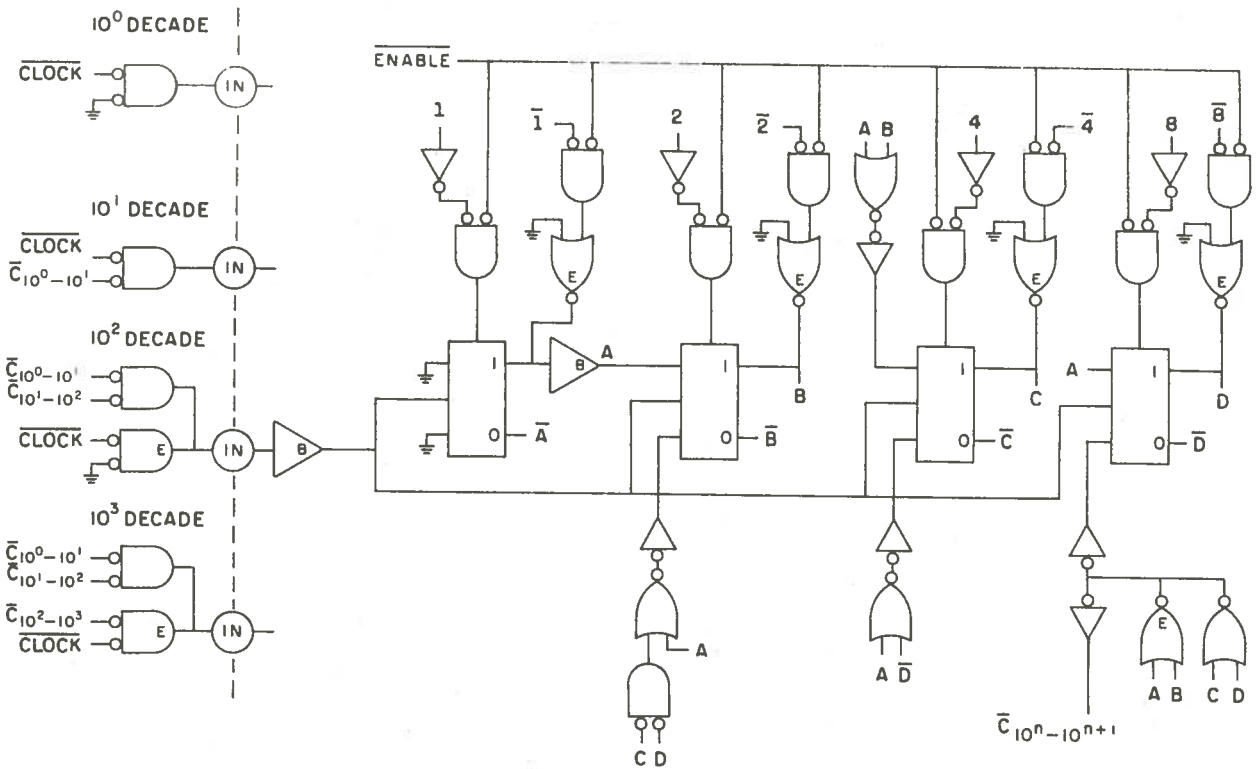
Figure 8 Clock down counter

The 100-kHz divider circuits are shown in Fig. 9. The drive signal to the clock down counter, $\overline{CLOCK}$, are 250-nsec pulses at either a 1000-Hz or 100-Hz rate. One of these pulse trains is selected by the front panel multiplier switch through either the ×1 enable or ×10 enable signal. A 500-nsec one-shot multivibrator sets up an inhibit to the "zero detect" circuit at each $\overline{CLOCK}$ pulse to prevent any false decoding. The modified latch circuit at the input to the divider circuits synchronizes the beginning of the clock interval to the next 100-kHz pulse following a monochromator generated readout. The six-decade counter is inhibited until the beginning of the clock interval by the $\overline{I}_{INHIBIT}$ signal (Fig. 5). Without synchronization there would be a 10-µsec ambiguity in the clock interval. The clock interval still will be approximately 1 µsec longer than set by the thumbwheel switches because of the delay in the ripple counters of the decade dividers. Differences between sample periods for the same time setting will be much less since changes will be due to incremental changes in logic element delays. The 100-kHz reference oscillator has a stability of better than 1×10^{-9}. The 100-kHz signal also has a high signal-to-noise ratio.
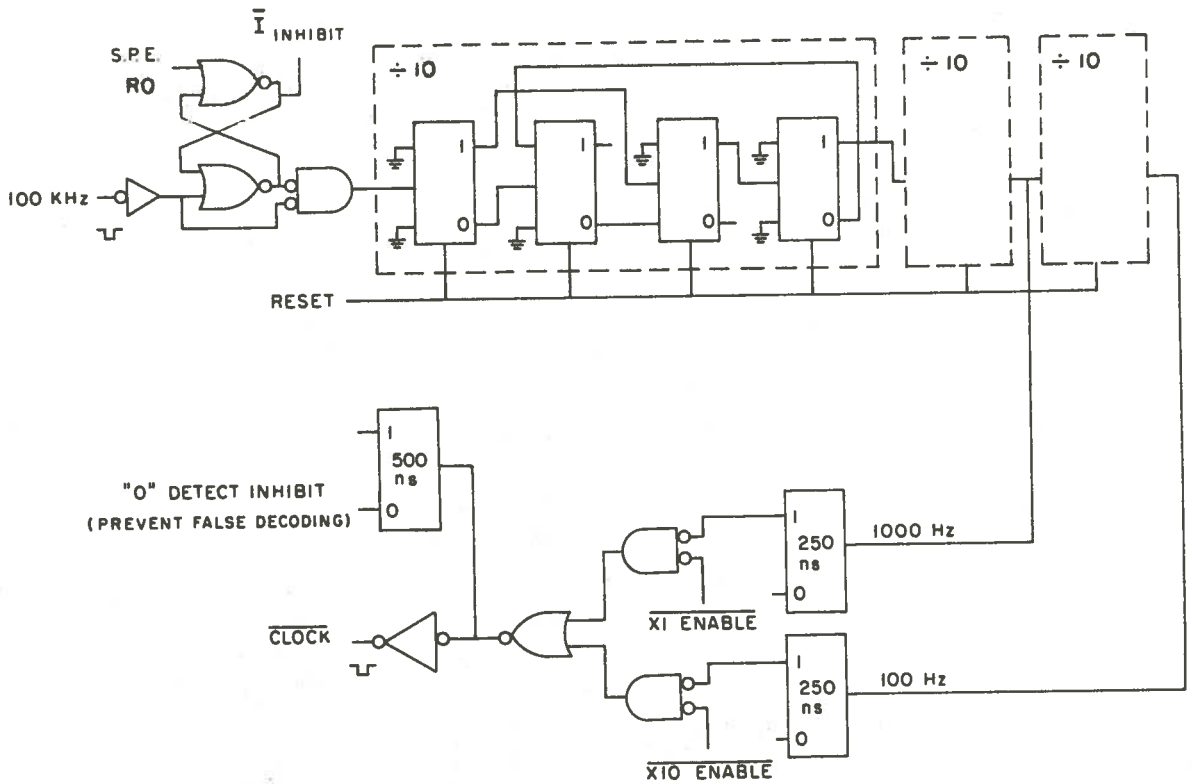
Figure 9 Divider circuits for 100 kHz reference

The circuitry to control the readout of the six-decade up-down counter is shown in Fig. 10. The clock determines the counting interval and the monochromator drive sets the sampling rate. At the end of the clock interval the count in the counter is stored in the output register and the counter is cleared, the clock is reset, and the counting cycle begins again. The monochromator drive initiates the recording of the data stored in the register. The monochromator drive readout command also clears the counter and resets the clock. Events occurring after a monochromator drive readout command are the same as at the end of a clock interval except that the contents of the storage register are unchanged.

In Fig. 10, a readout command (the $\overline{R}$ signal) is generated either at the end of a clock interval, when the clock has been decremented to zero, or by a monochromator drive readout command ($\overline{RO}$). However, if $\overline{R}$ results from an $\overline{RO}$ signal then the $\overline{S}_{INHIBIT}$ signal is generated to prevent the register from being strobed. The inhibit on the register strobe is removed by the next clock generated readout pulse. If the monochromator drive readout command and clock generated readout command occur together, the clock generated command dominates, that is, the counter data are transferred to the counter storage register. The output of the coincidence latch prevents the $\overline{S}_{INHIBIT}$ from being raised. The strobe signal $\overline{S}$ resets the latch.
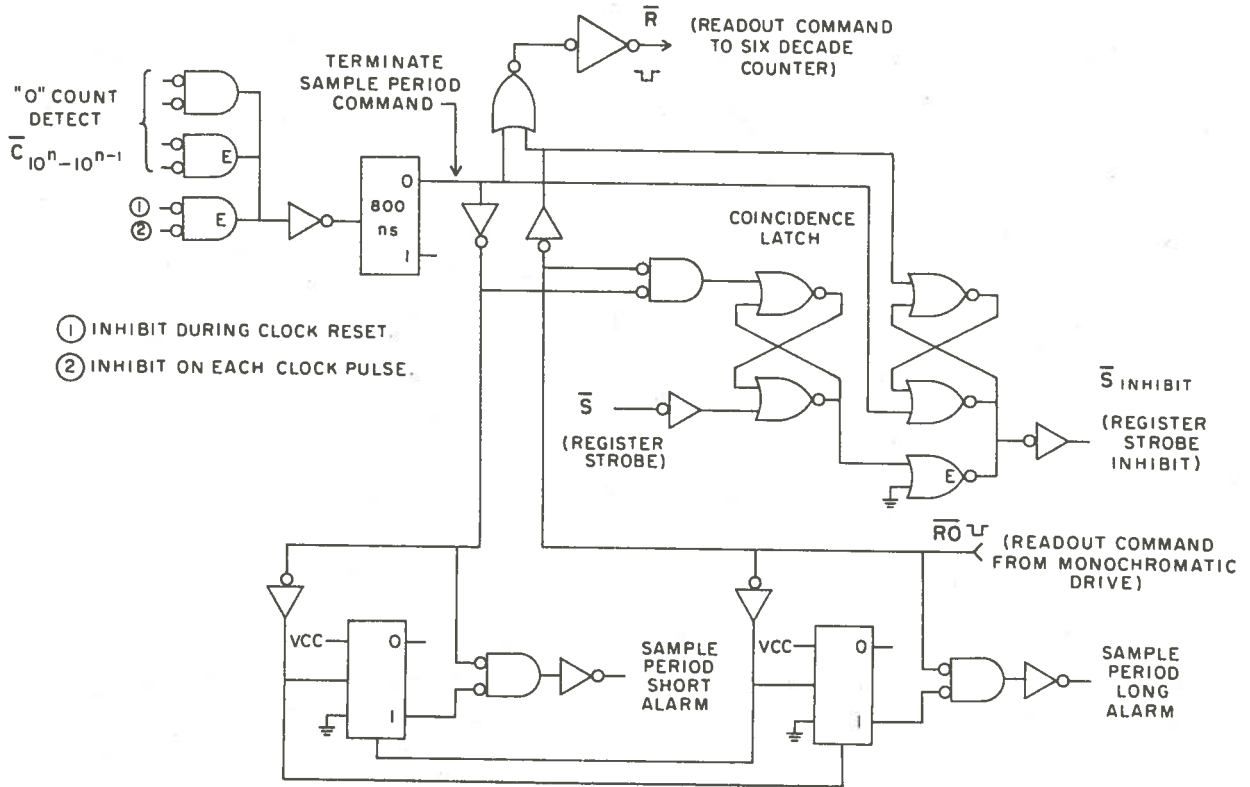
Figure 10 UP-DOWN counter readout control

Also shown in Fig. 10 are the sample-period-short alarm and sample-period-long alarm detection circuits. The sample-period-short alarm is triggered if two clock generated readout commands occur in sequence without a monochromator drive readout command interspacing them. The trailing edge of the clock generated readout command pulse triggers the flip-flop which then enables the AND gate. The next clock generated readout command pulse will be passed by the AND gate to trigger the alarm unless the flip-flop has been set by the monochromator readout command pulse. The sample-period-long alarm circuit is similar to the other alarm circuit except that the input signals are interchanged.

Interface Circuits

The counter and clock circuits use digital integrated circuits with signal levels nominally 3.5 volts and 0 volts. The output from the preamplifier-discriminator is the only interface signal which matches the integrated circuit levels. Therefore, all the remaining input/output signals must undergo level conversion at least. The 100-kHz reference signal to the clock is a 40-volt peak-to-peak sine wave. A schmitt-trigger type circuit, Fig. 11, located in the unshielded part of the chassis, changes this wave into a 6-volt square wave. The
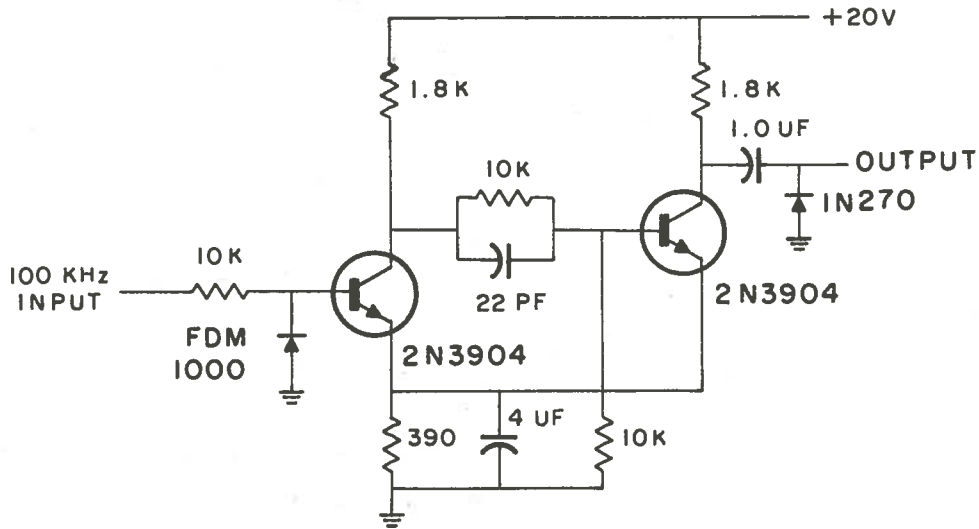
Figure 11 100 kHz reference shaping circuit

square wave is further shaped on board No. 1 into nominal 3-volt, negative going, 220-nsec pulses before input to the clock in Fig. 9.

The monochromator readout pulse is a nominal -6 volt pulse. The circuit shown in Fig. 12 generates an 800-nsec negative going pulse which is the $\overline{RO}$ signal in the clock control circuits in Fig. 9. A level changer circuit for the BCD output from the storage register is shown in Fig. 13. The output levels are 0V and -6V for 3V and 0V input.
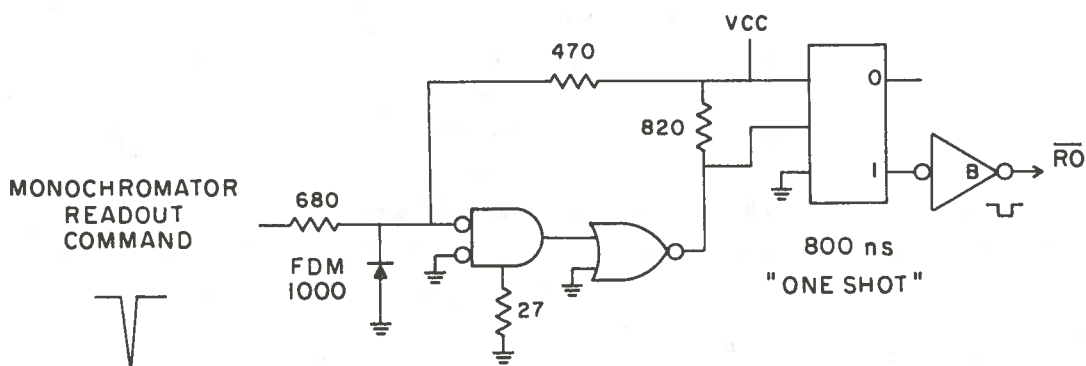

Figure 12 Monochromator readout command shaping circuit

At the time of writing the up-down control interface has not been built because the type of chopper to be used has not been decided upon. Space has been left on board No. 1 for the necessary interface circuits.
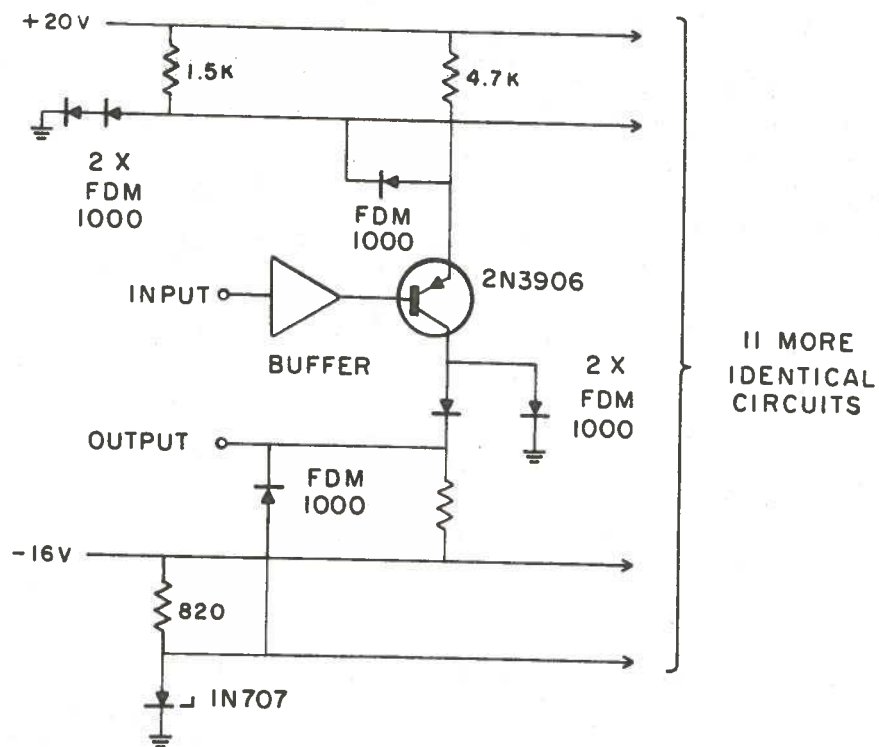
Figure 13 Level change circuit for output data

Figure 14 shows the circuit of the digital-to-analog converter. Output resolution is 1% and inputs may be switched between the upper two or lower two decades of the storage register. The resistor values shown on the ladder network are nominal. Buffers and resistor values were matched to provide the equivalent of the nominal values. Strip-chart calibration was easily accommodated since the input buffers are OR gates. During calibration normal signal inputs are grounded and the alternate inputs on the most significant decade are switched to give 0, 0.1, 0.5 and 0.9 of full scale indications.

Physical Layout

All integrated circuits are mounted in a metal enclosure as shown in Plate II. Power supply lines are filtered as they enter the shielded area, signal lines are not filtered. In general, these signal lines are less susceptible to noise since they have large voltage swings (6V for the BCD coded outputs). In addition, the counter low-level circuits are partially isolated by the interface circuits. Both the monochromator readout command pulse and 100-kHz reference signal detection circuits have thresholds greater than 5 volts. The high-level signal lines have been carefully dressed away from counter circuits to avoid coupling noise into the counter.
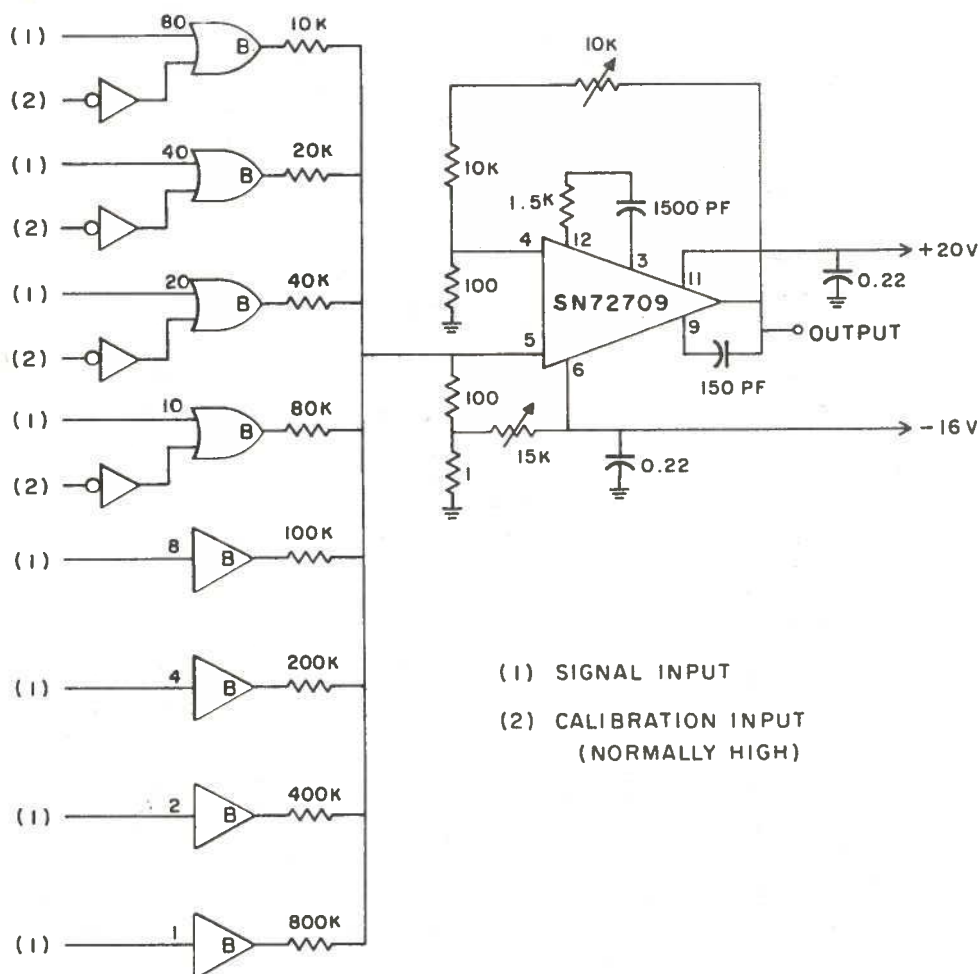
Figure 14 Digital-to-analog converter

Both the counter range switch and the clock preset switches are mounted outside of the enclosure. Twisted pairs are used for these control lines and external paths are kept short.

Both ground and V_{cc} buses are heavy conductors to provide a low impedance power supply. To further reduce self-generated noise and other noise on the power supply, V_{cc} is by-passed to ground at each printed circuit board with a 0.01-μF capacitor. Each board has a copper bus around the edge which is at ground potential. Circuit ground is connected to chassis ground at one point only.

Wiring between printed circuit boards was considered most vulnerable to noise pickup. Function allocation to circuit boards has been grouped to minimize interconnections. If an interconnecting

signal has a quiescent state, then this state is transferred at a high level to take advantage of the increased noise margin at the positive or high level of RTL logic. An example of a signal with a definite quiescent state is the buffer strobe ($\overline{S}$). The strobe signal is a 100-nsec pulse which occurs at 50-msec intervals or greater. (Assymetry ratio of 5×10^5) Reduced circuit loading (low fanout) further raises the absolute voltage of the high level, so increasing the noise margin. Further improvement in noise immunity is available if a buffer amplifier is used, first owing to the greater voltage swing, but also owing to the lower output impedance of the "totem pole" circuit of the buffer amplifier.

Reference

1. Cairns, F.V. and Bechthold, G. Digital data recording system for luminescence spectra. NRC Report ERB-746, October 1966.

Detail wiring drawings on file in the drawing office of the Radio and Electrical Engineering Division, NRC

DS-11-1E   6 Decade BCD Up/Down Counter
DS-11-2C   Block Diagram
DS-11-3E   Sample Period Control Circuits
DS-11-4E   Systems Interface Control Circuits
DS-11-5D   Power Connector and Discriminator
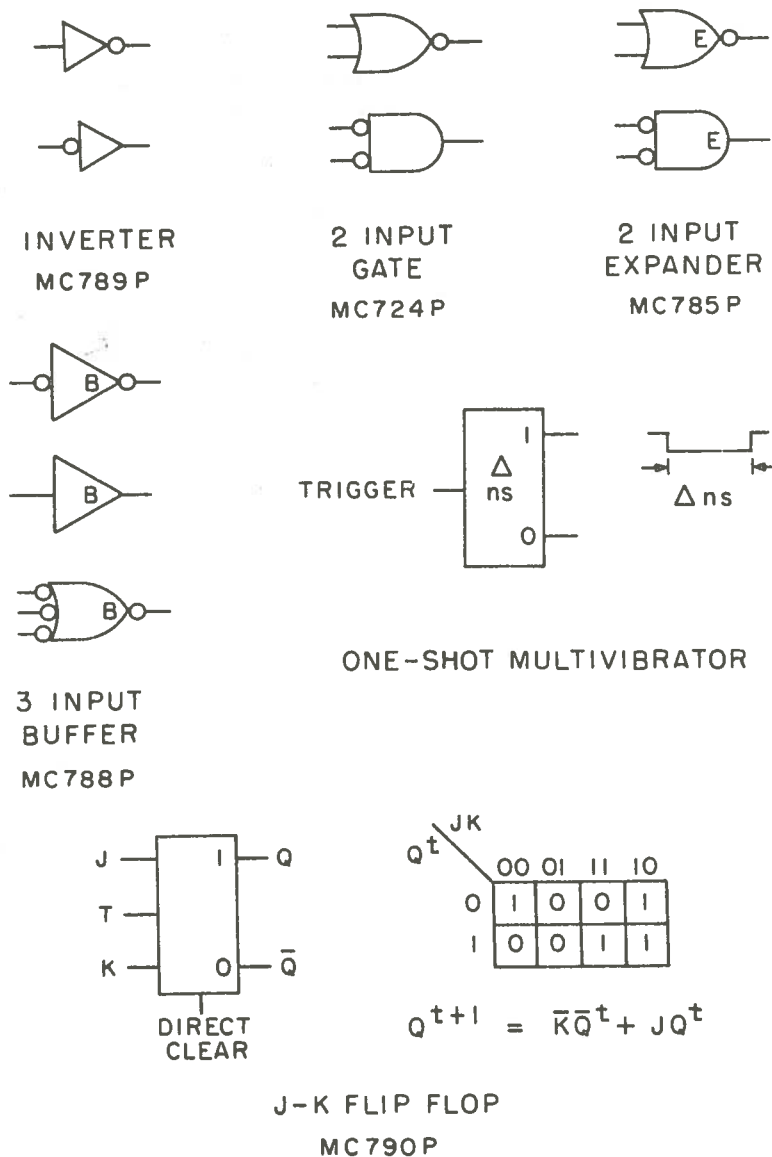DS-11-6D   Integrated Circuit Package Layout

INVERTER
MC789P

2 INPUT
GATE
MC724P

2 INPUT
EXPANDER
MC785P

3 INPUT
BUFFER
MC788P

TRIGGER

ONE-SHOT MULTIVIBRATOR

$Q^{t+1} = \bar{K}\bar{Q}^t + JQ^t$

J-K FLIP FLOP
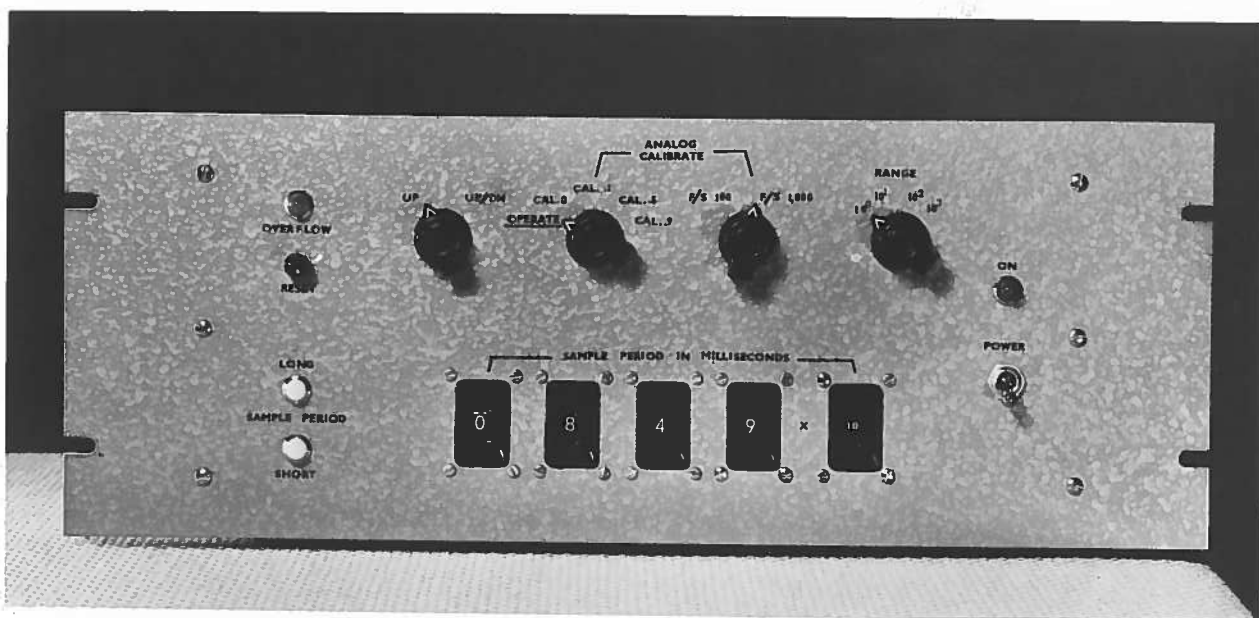MC790P

Figure 15 Symbol identification
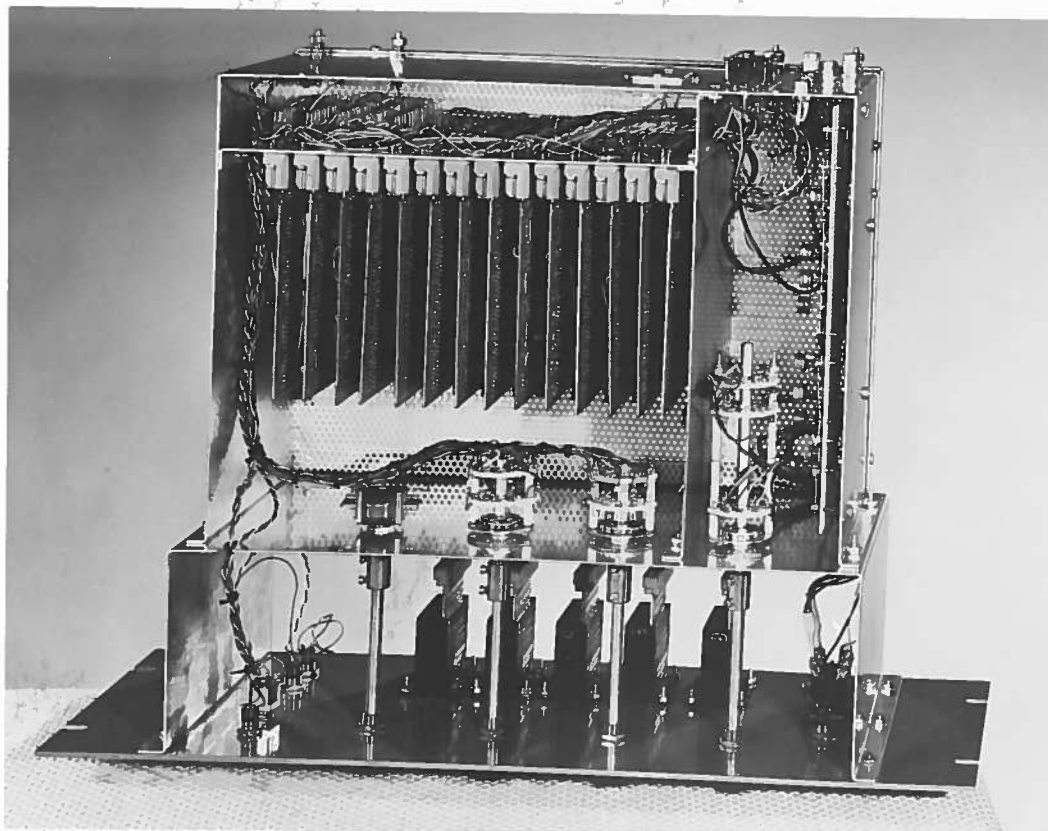
Plate I   Front panel layout of counter

Plate II   Counter chassis showing shielded section for integrated circuits