Development of inkjet-printed inverters

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NRC·CNRC

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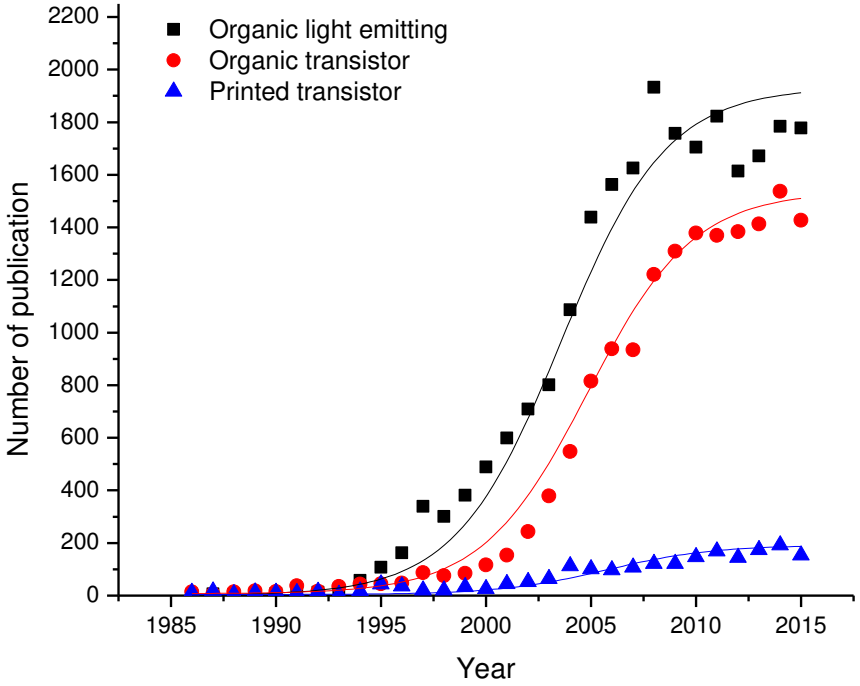
Outline

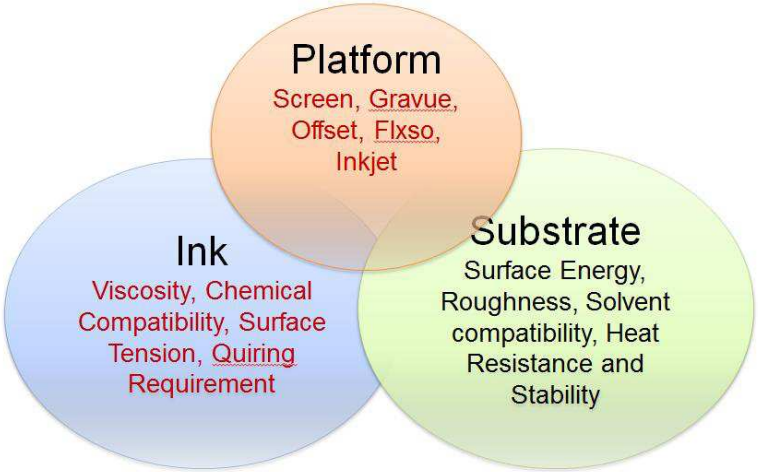
- Introduction
- Development of 3-layer-printed OTFTs
- Different types of printed inverter developed at NRC
  - Enhancement-load PMOS inverter
  - PMOS inverter (screen printed resistor)
  - CMOS inverter
- Stability of printed inverter

Challenges in printing process



Challenges → yield, stability

- **Uniformity, Roughness**
- **Interface interaction**
- **Solvents compatibility**
- **Drying process**
- **Printing platform**

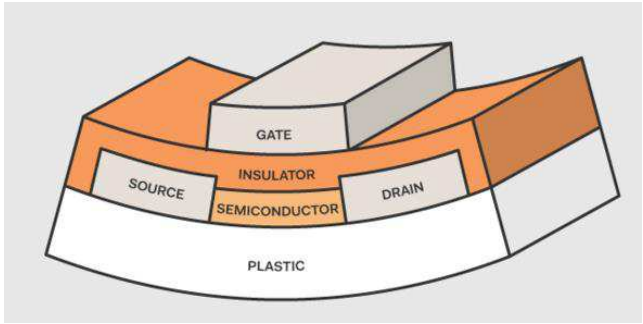


Thermal evaporation
Spin coating

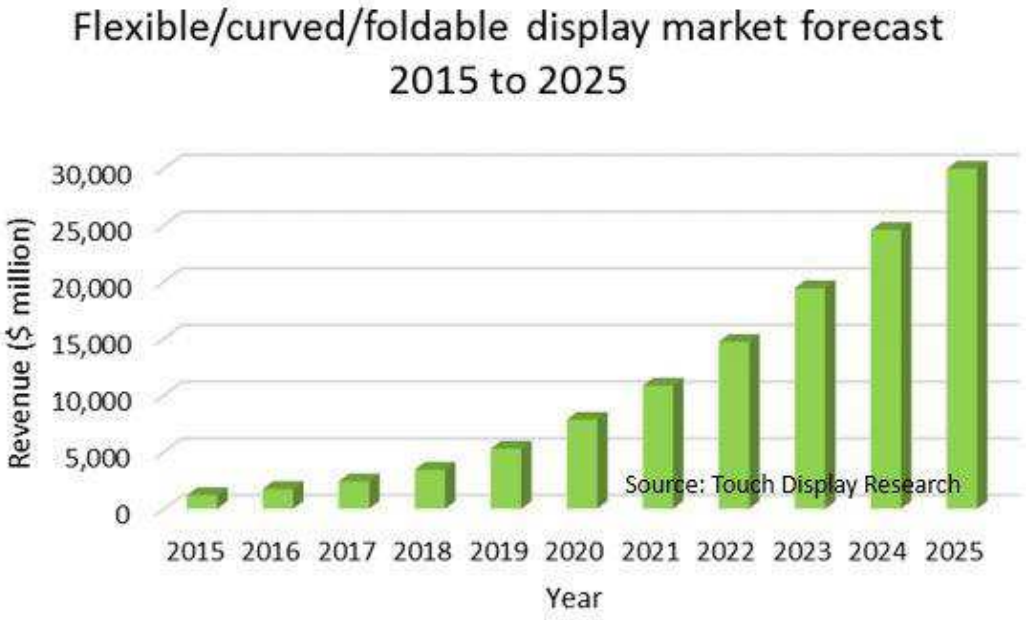
Printing process

Polymer based transistor backplane is required for flexible/bendable electronics in the future

Polyera smartwatch using OTFTs



Flexible→ Curved→ Foldable→ Bendable



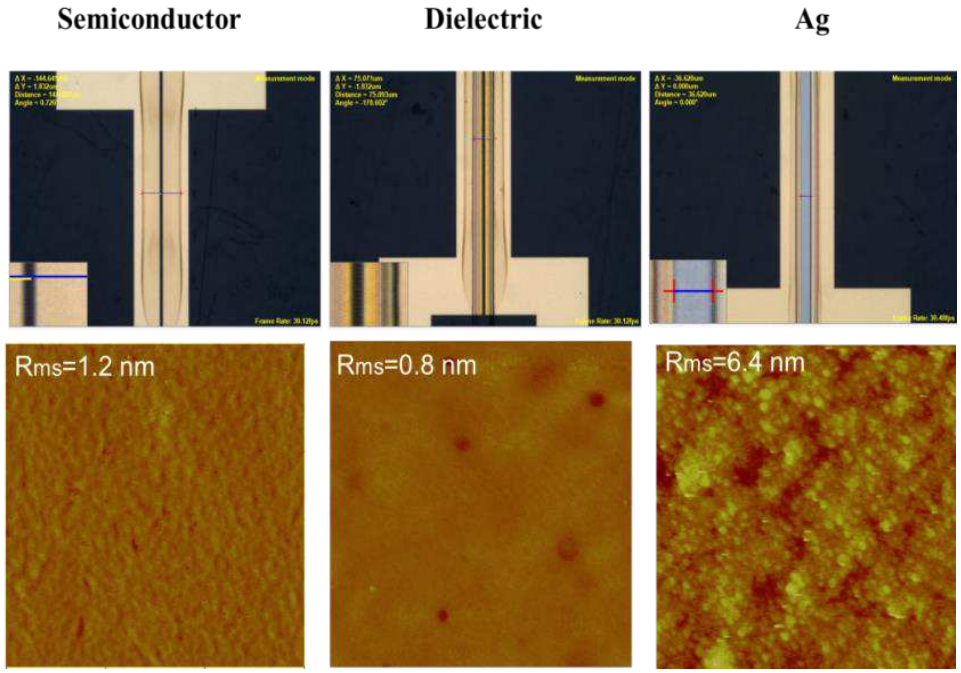
Spin coated dielectric and sputtered gate electrode

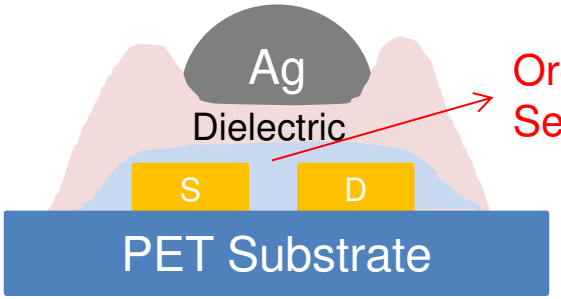
NRC 3-Layer-Printed Organic Thin Film Transistors (OTFTs)

- ✓ No spin coating process
- ✓ Printing process in ambient air

Inkjet printed layers

- ➢ Organic semiconductor
- ➢ Dielectric
- ➢ Ag top gate electrode

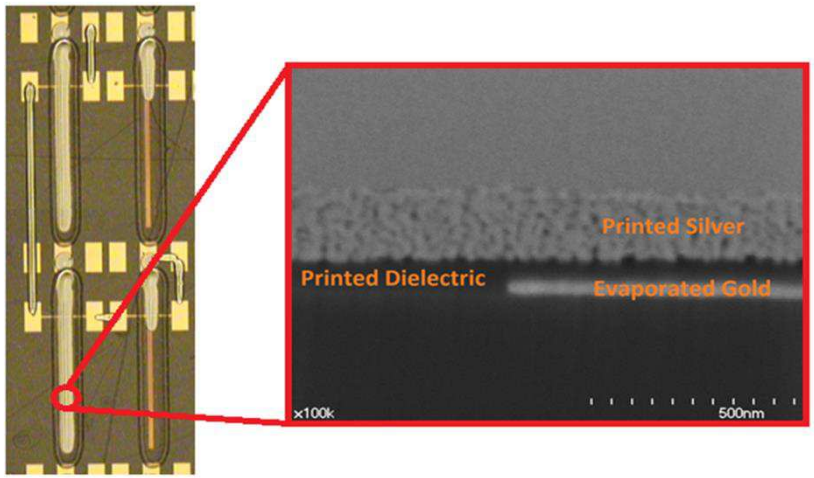




3-layer-printed OTFTs

Thin and uniform printed dielectric layer enabled by the coffee ring effect

- Transistor driving voltage is proportional to the thickness of dielectric layer
- Difficult to achieve a pin-hole free of thin dielectric layer by printing method
- Coffee ring effect is usually undesirable



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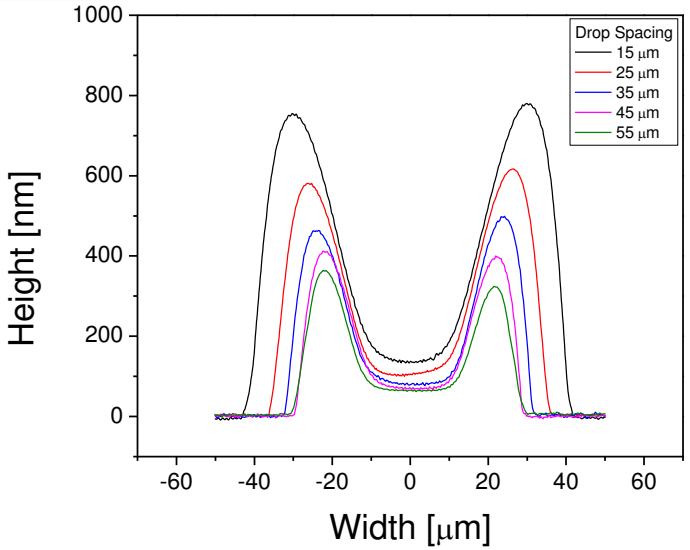
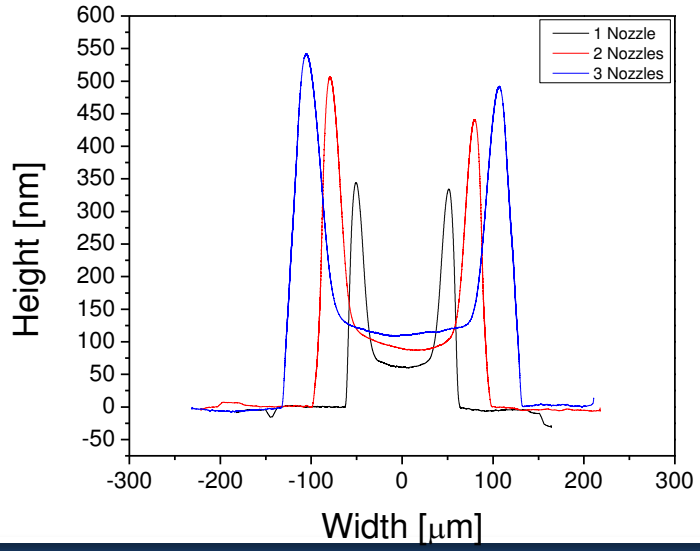
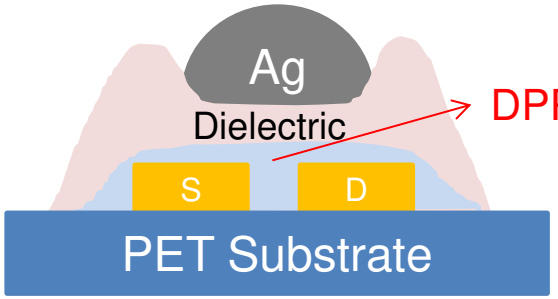
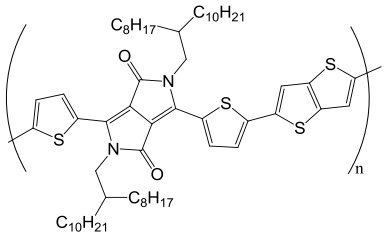




3-layer-printed OTFTs mobility up to ~1 cm²/Vs at 15 V



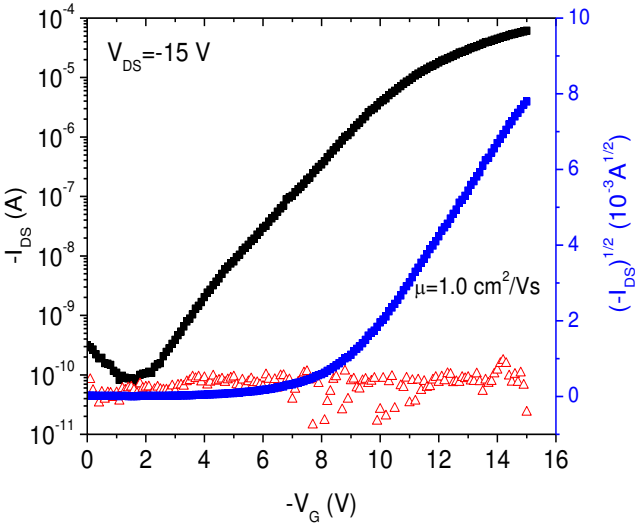
DPP-DTT

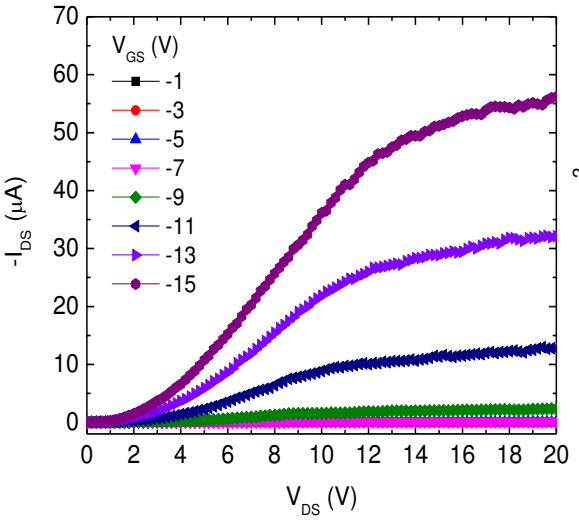


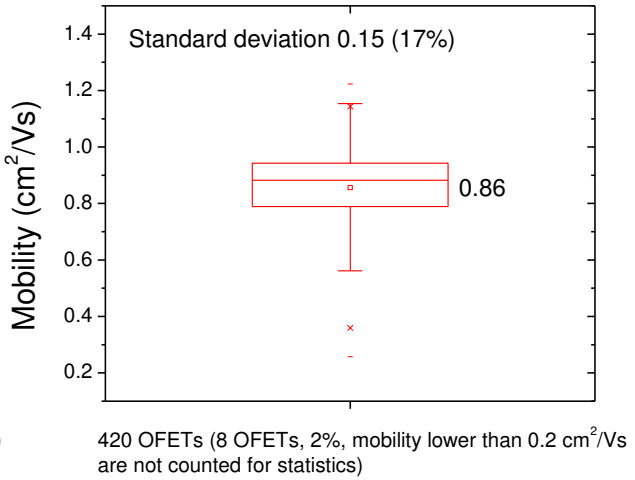
Dielectric thickness~ 250 nm
Max. Processing Temp. 140°C

3-layer-printed OTFTs

Average mobility of 0.86 cm²/Vs (variation σ~15%) with on/off ratio of 10^5 obtained at 15 V.





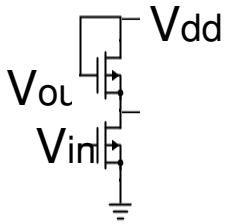


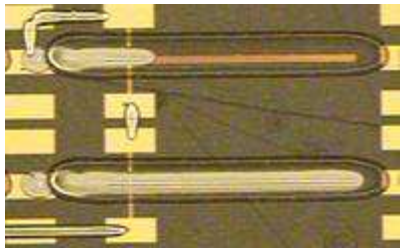
420 OFETs (8 OFETs, 2%, mobility lower than 0.2 cm²/Vs are not counted for statistics)

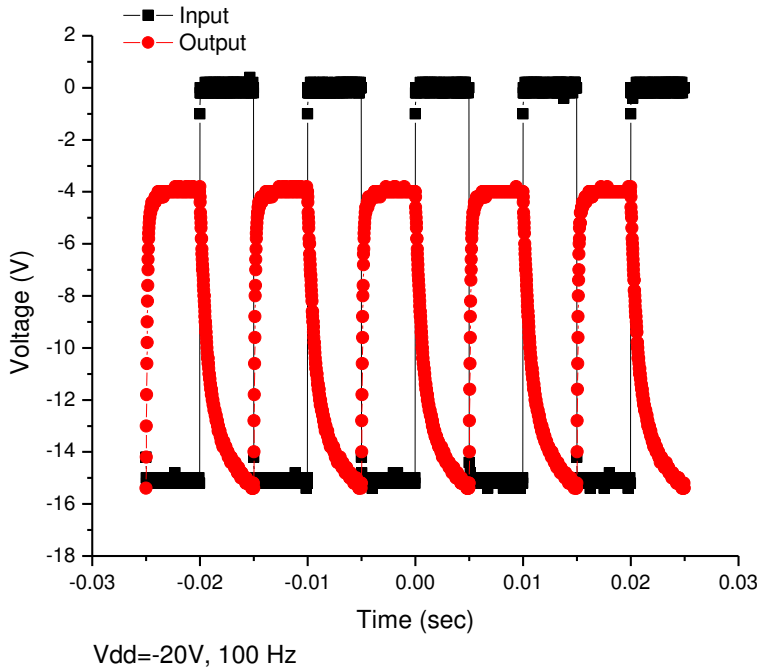
Channel length 5 μm, channel width 1 mm

Printed PMOS enhancement-load Inverter and relative logic circuits

Simplest printing process and excellent stability
Lower output amplitude







Vdd=-20V, 100 Hz

Channel length L= 5 µm,
Channel width

- Drive transistor W=1 mm
- Load transistor W=200 µm,

Printed logic gates NAND, AND, NOR and OR

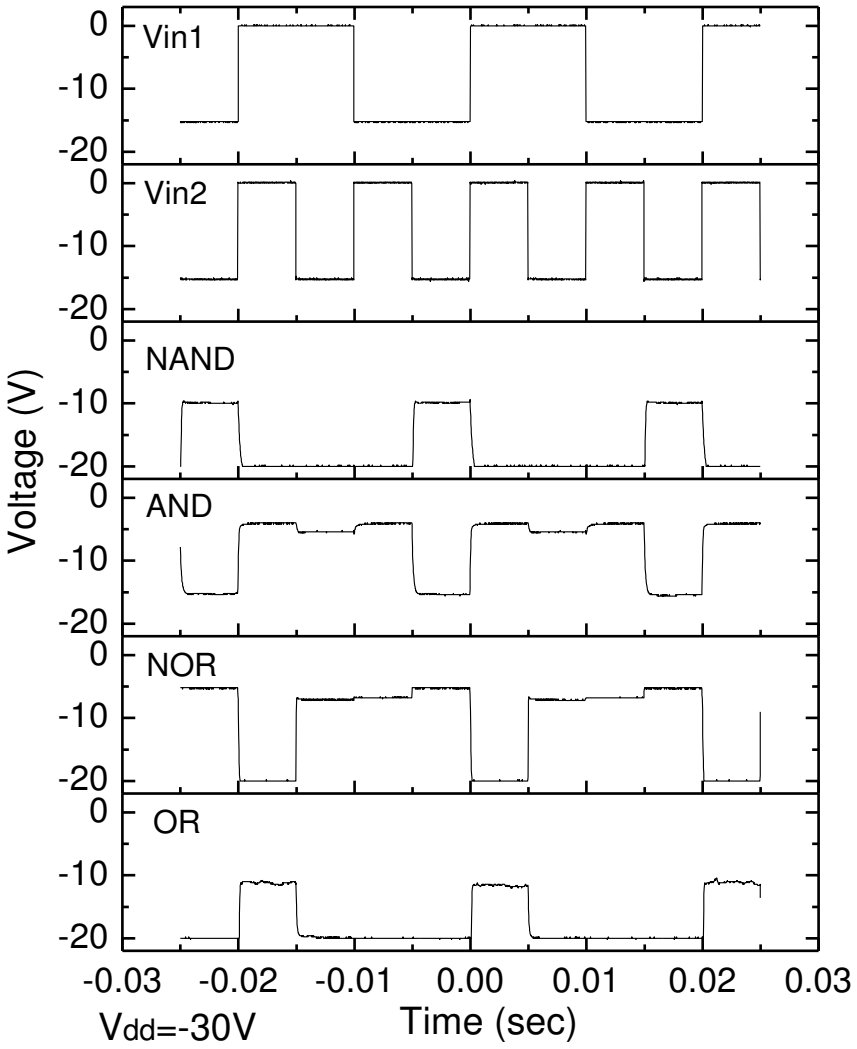
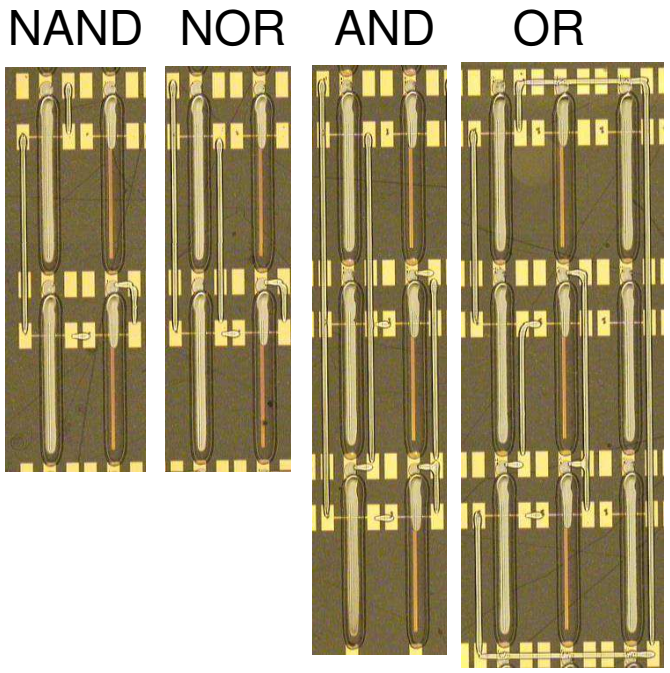
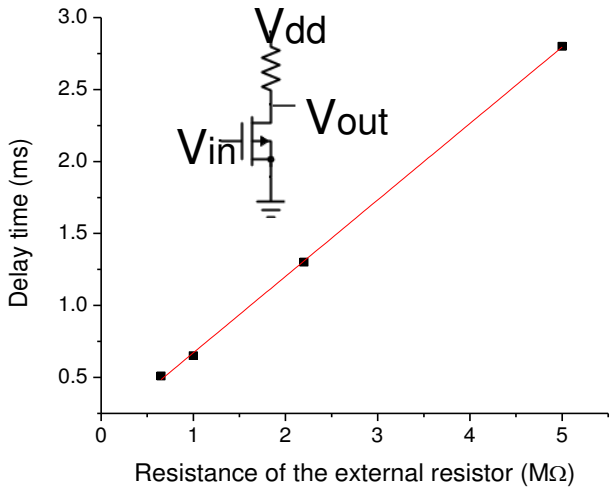


Table 1. Truth tables for NAND, AND, NOR and OR logic gates

		Output for the different logic gates			
Vin 1	Vin 2	NAND	AND	NOR	OR
1	1	0	1	0	1
1	0	1	0	0	1
0	1	1	0	0	1
0	0	1	0	1	0

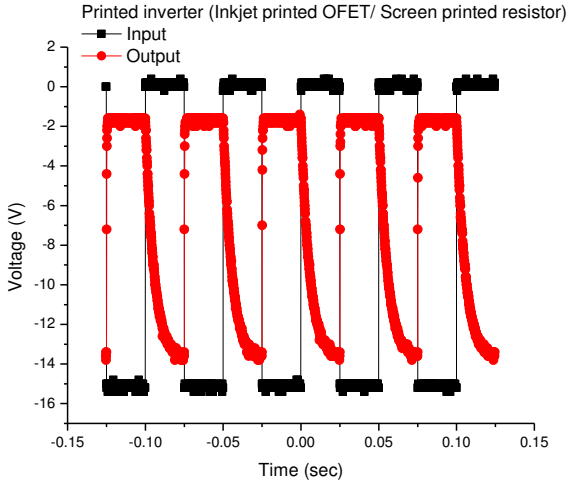


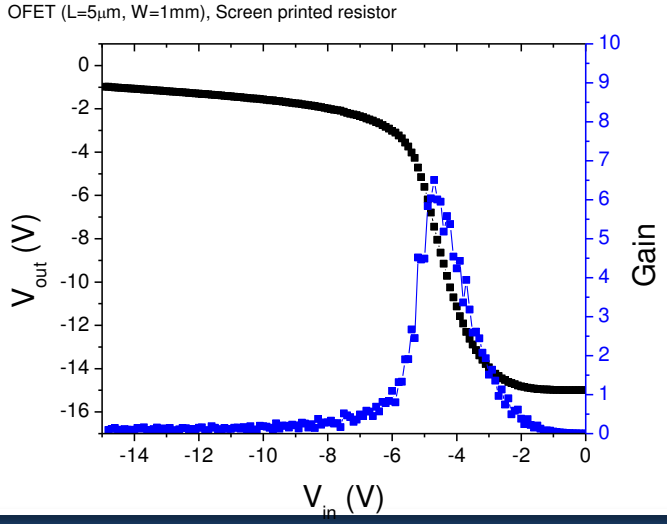
Printed PMOS inverter using screen printed resistor



Delay time is dominated by the resistance

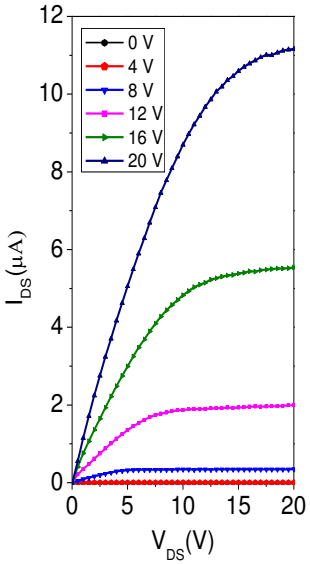
Screen printed carbon ink for resistor

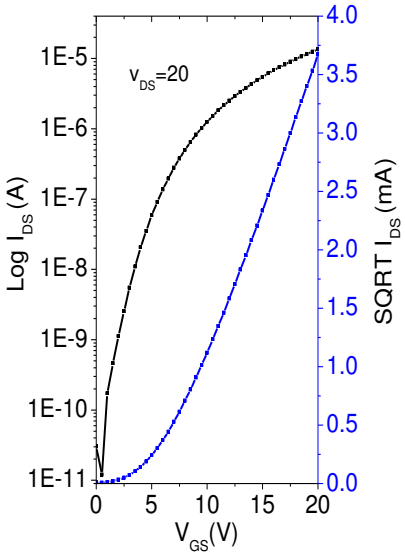


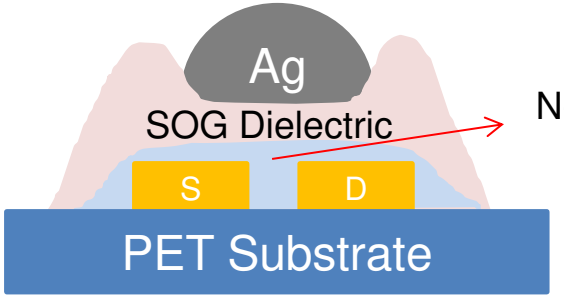


Development of printed CMOS inverter

3-Layer-Printed N type transistor

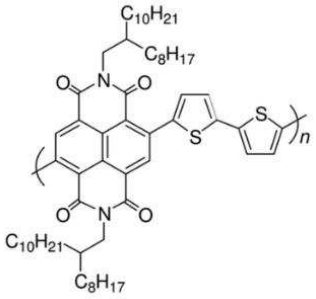






3-layer-printed OTFTs

NDI2OD-T2
N-type semiconductor



Dielect. Thick. (nm)	Mobility (cm^2/Vs) @ bias=20 V	V_{th} (V)	On-current (A)	Off-current (A)	On/Off
800	0.01	12.8	2.5E-07	1.16E-12	2.1E+05
450	0.05	10.9	3.2E-07	1.20E-12	2.6E+05
300	0.05	9.7	5.0E-07	7.15E-12	7.0E+05
220	0.10	8.4	8.8E-06	6.24E-11	1.4E+05
180	0.12	4.1	1.5E-05	6.70E-10	4.0E+04

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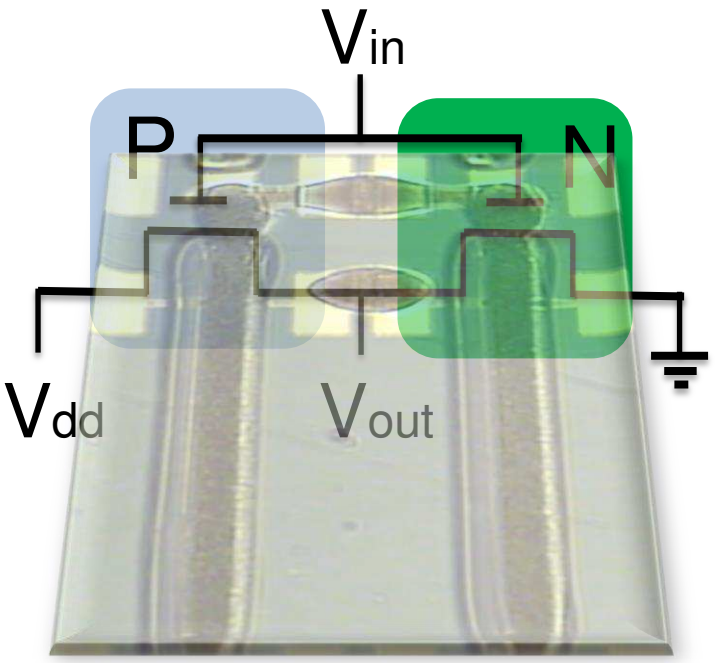
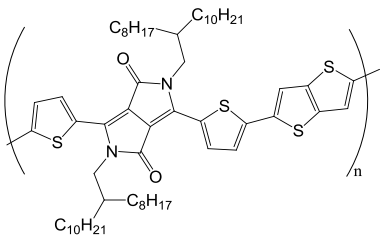
Development of printed CMOS inverter

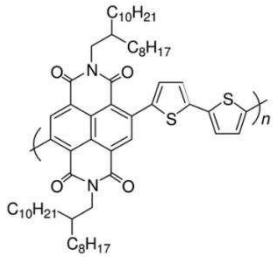
Difficulties

- Compatible processing condition for both P and N type materials
- Compatible IV characteristics
- Stability between P and N

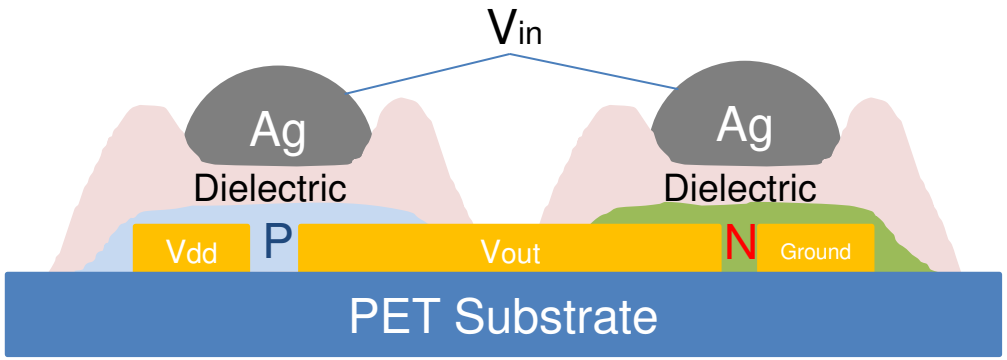




DPP-DTT
P-type semiconductor

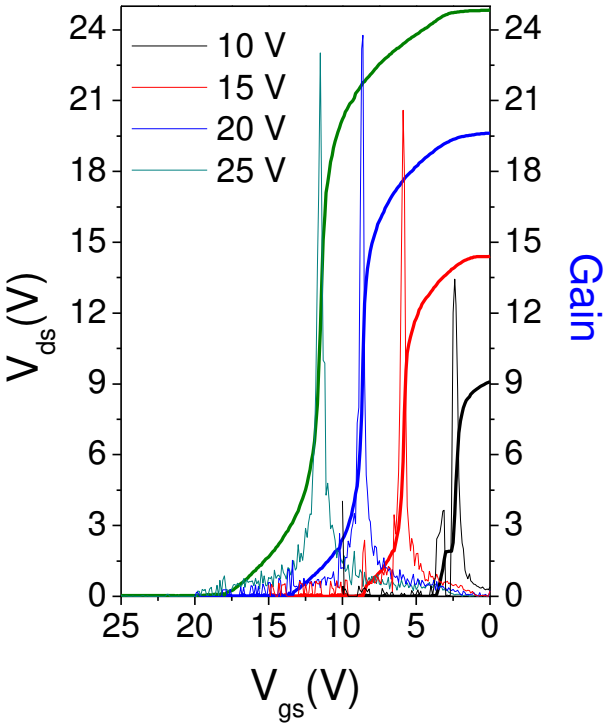


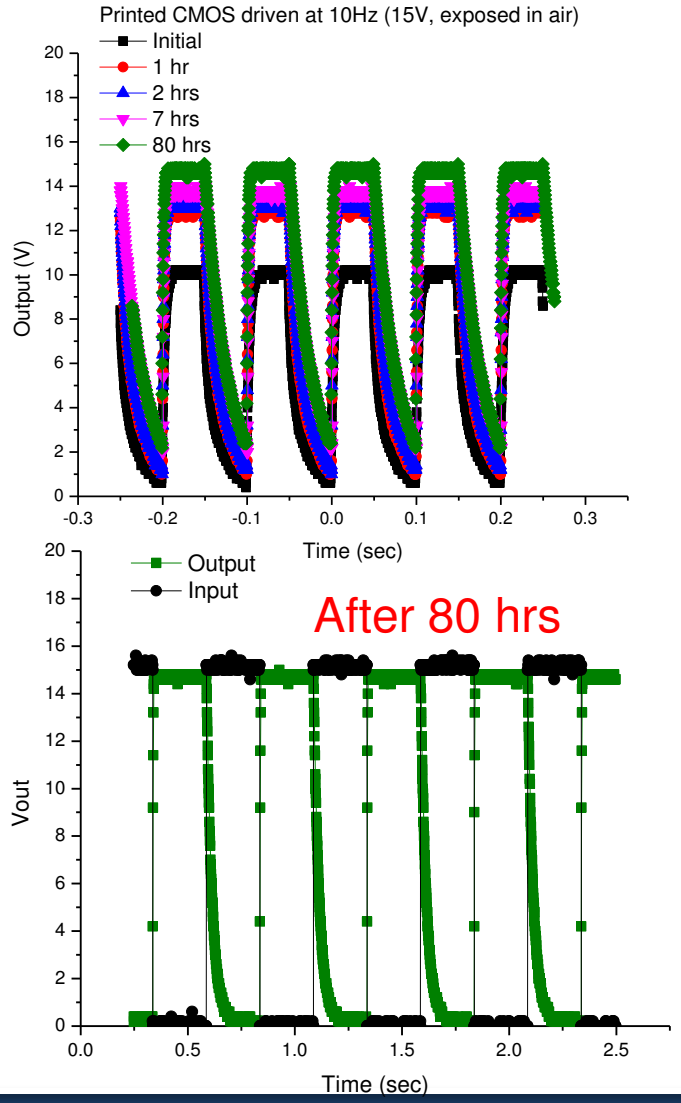
NDI2OD-T2
N-type semiconductor



Development of printed CMOS inverter

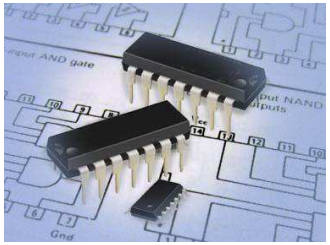
- Full-swing output amplitude achieved
- Gain value of 24 obtained
- Air stability testing without encapsulation

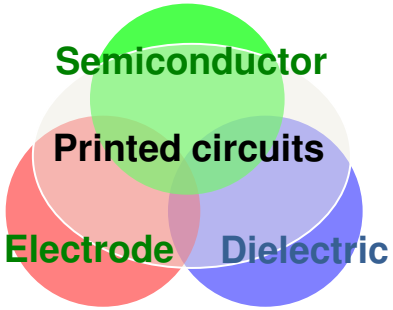


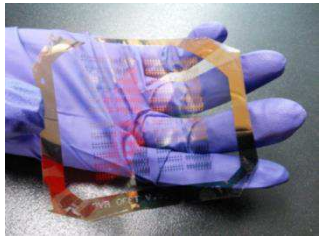


Summary

- NRC developed printing process for 3-layer-printed OFETs, mobility of 1 cm^2/Vs on PMOS and 0.1 cm^2/Vs on NMOS transistors have been achieved.
- Introduced coffee ring effect to achieve thin and uniform dielectric layer by inkjet printing process.
- Gain value of 24 with a nearly full-swing of output voltage obtained from the printed CMOS inverter.
- Demonstrated the air stable printed CMOS without encapsulation







Printed logic circuits for electronics integration

Thank you for your attention!

Question?

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