BIRIS accelerator Video Digitization Board: hardware specifications: VDB Rev. 1

Mario, Lecavalier; François, Blais

https://doi.org/10.4224/23000139

National Research Council Canada
Conseil national de recherches Canada

Limited distribution

Institute for Information Technology
Institut de technologie de l'information

NRC·CNRC

BIRIS Accelerator Video Digitization Board Hardware Specifications VDB Rev. 1

M. Lecavalier and F. Blais
January 1995

Canada

NRC 38366

BIRIS Accelerator Video Digitization Board
Hardware Specifications
VDB Rev. 1

Mario Lecavalier and François Blais
January 1995

Table of Contents

1. *Introduction*

The BIRIS accelerator minimum configuration consists of three separate boards. The first module is the Video Digitization Board (VDB), the second is the Digital Processing Board (DPB), and the third is the Transputer Mother Board. This document describes the VDB hardware functional specifications.

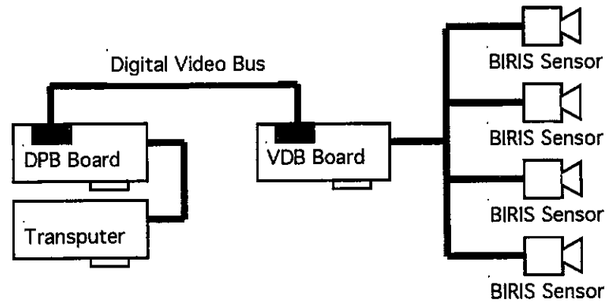
The Video Digitization Board is the interface system between the BIRIS sensor cameras and the Digital Processing Board. Its mission is to convert the analog video signal amplitude into a 12-bit digital code and then send this information to the DPB for processing. The maximum digitization sampling rate is 10 MHz and is programmable.

The VDB accepts up to four BIRIS sensor video signals but only one is selected at any time. The VDB extracts the synchronization signals from the analog video of the selected sensor. Through software configuration, the VDB accepts standard video formats such as RS170A and CCIR. Nonstandard video signal may be acceptable but will require a specific analysis.

A programmable SYNC generator is imbedded into the design so the VDB can provide the Horizontal Drive (HD) and Vertical Drive (VD) necessary to synchronize several BIRIS sensors.

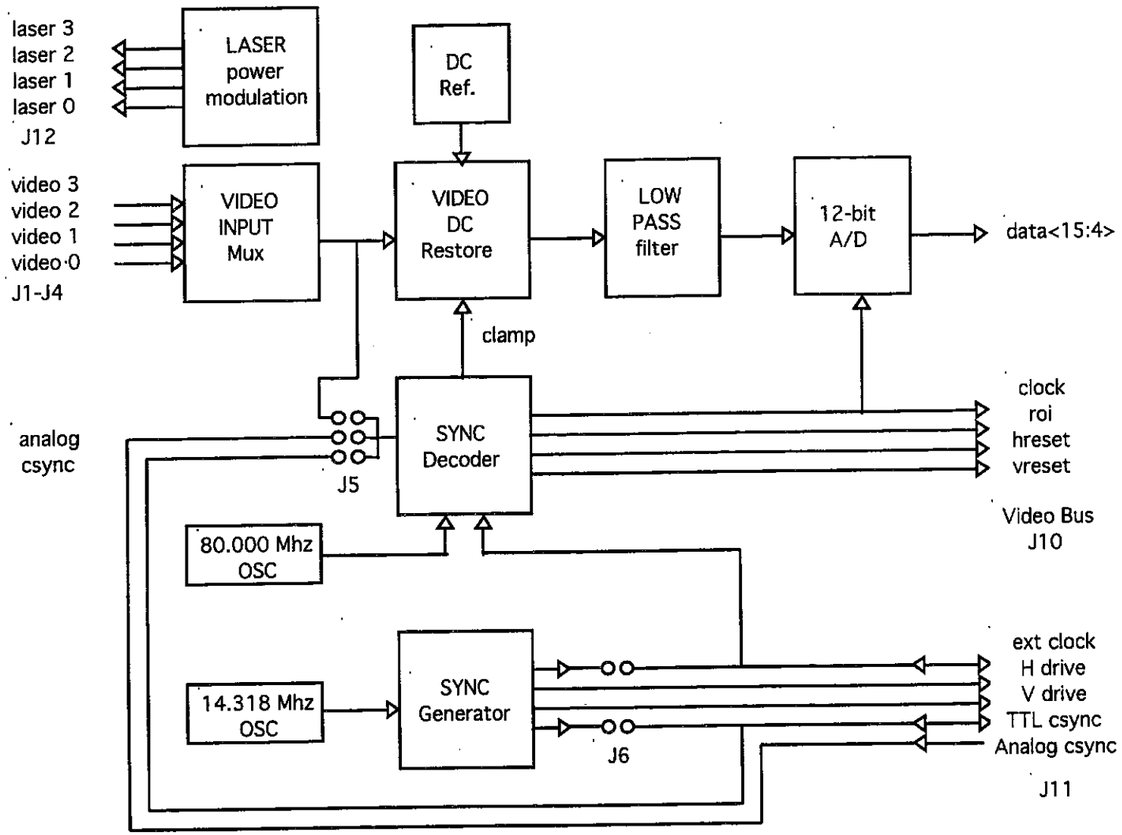
Also, four TTL outputs with individual programmable duty cycles are available to modulate the laser emission power of each BIRIS sensor. Only the laser power of the selected BIRIS sensor will be modulated; the other three modulation signals will be inactive.

All the VDB hardware resources are initialized through the Digital Video Bus by the DPB. There is no need for any PC/AT bus interface on the VDB and, thus, the VDB takes only its power supplies from its host computer. The VDB is a full-sized PC/AT board and occupies a single slot in the computer chassis.



The BIRIS accelerator system

1.1 VDB Block Diagram



2. *The Digital Video Bus Interface*

The Video Bus serves a dual purpose in the BIRIS accelerator system. First, the Video Bus is used to program registers on a remote slave VDB module and, second, it is used to transfer digital pixels at video rate from the VDB to the DPB.

2.1 Registers Programming Mode

The VDB does not have a local CPU and is a slave module to the Video Bus. After a power-up, the VDB main functions are disabled and the board monitors the Video Bus for a register cycle to one of its resources.

The VDB occupies 16 consecutive address locations from the 256 available with the 8-bit address bus driven by the Video Bus master. Four configuration straps located on the jumper block J8 can map the VDB register set on any 16 locations boundary. This address offset is called the VDB Registers Base address.

For the VDB Registers Base address strapping information, see the complete description of J8 in Appendix A.

The Video Bus provides an 8-bit data path for registers programming and all the VDB hardware resources are 8-bit wide.

2.1.1 *Mapping of VDB Registers*

Address	**Register name**	**Attributes**
0	Control Register 0	Write only, 0 Wait state
1	Status Register	Read only, 1 Wait state
2	Bt261 Address Register	Read 1 WS, Write 0 WS
3	Bt261 Data Register	Read 1 WS, Write 0 WS
4	LM1882 Address Register	Write only, 0 Wait state
5	LM1882 Auto Load Mode	Write only, 0 Wait state
6	LM1882 Low Byte Data Register	Write only, 0 Wait state
7	LM1882 High Byte Data Register	Write only, 0 Wait state
8	Vertical Look-up Table (VLUT) Data Register	Read 2 WS, Write 2 WS
9 - 15	Unused	

2.1.2 *Descriptions of VDB Registers*

Control Register 0

address: VDB base + 0.
attributes: Write only, 0 wait state.
power up value: 0xFF.

bits <1:0> Video channel select.

00 = Select video channel 0 and activate laser TTL modulation 0.
01 = Select video channel 1 and activate laser TTL modulation 1.
10 = Select video channel 2 and activate laser TTL modulation 2.
11 = Select video channel 3 and activate laser TTL modulation 3.

bit 2 Laser disable.

0 = Activate the TTL modulation signal of the selected channel.
1 = Deactivate all TTL modulation signals. Depending on the configuration jumper block J6 pins 7-8, a static TTL low or high voltage will be output on the four modulation signals of J12.

bit 3 Video Bus disable.

0 = Enable the TTL drivers of the VDB board to drive the Video Bus signals related to the video acquisition (DATA<15:0>, PCLK, ROI/, HRESET/, VRESET/, FIELD). Only one VDB board can drive the Video Bus at any time.
1 = Disable the TTL drivers of the VDB board to drive the Video Bus signals related to the video acquisition (DATA<15:0>, PCLK, ROI/, HRESET/, VRESET/, FIELD).

bit 4 VLUT programming.

0 = Normal video acquisition mode. The vertical LUT is addressed with a counter incremented on each HRESET/ pulse.
1 = VLUT programming mode. The vertical LUT is addressed with a counter incremented after each read or write cycle to the VLUT.

bit 5 VLUT address counter reset.

0 = The VLUT address counter is free to count.
1 = The VLUT address counter is reset to zero.

bits <7:6> Video channel selection mode.

00 = **Mode 0** The video channel is selected from the two bits value stored in the VLUT bit <7:6>. This mode allows the switching of video channels during an active frame at the beginning of any arbitrary horizontal video line. It is then possible to create a single video frame mosaic containing sections of the video information of several (synchronized) cameras.

01 = **Mode 1** The video channel is selected from the two bits <1:0> of this register. The two bits are synchronized with the next VRESET/ falling edge. This mode relaxes the CPU to update the video channel selection any time during the video vertical frame.
10 = **Mode 2** Same as Mode 1 plus the VLUT bit 6 is routed to the VERT_INTERRUPT on the Digital Bus. This allows the interrupt assertion at the beginning of any arbitrary horizontal video line.
11 = **Mode 3** The video channel is selected directly from the two bits <1:0> of this register. This is the default mode after power up for backward compatibility with the VDB Rev 0. Also, this mode is require to exit from a deadlock condition that may occur when a video channel without camera signal is selected. Remember that to generate a VRESET/ a video signal must be decoded and without VRESET/ the Modes 0, 1, and 2 are frozen.

See Section 4.1 for more details.

Status Register

address: VDB base + 1.
attributes: Read only, 1 wait state.

bits <1:0> Current video channel selected.

00 = Video channel 0 selected and laser TTL modulation 0 activated.
01 = Video channel 1 selected and laser TTL modulation 1 activated.
10 = Video channel 2 selected and laser TTL modulation 2 activated.
11 = Video channel 3 selected and laser TTL modulation 3 activated.

bits <7:2> Undefined.

See Section 4.1 for more details.

Bt261 Registers

Consults the Data specifications of the Bt261 from Brooktree.

LM1882 Registers

Consults the Data specifications of the LM1882 from National Semiconductor.

Vertical Look-up Table (VLUT) Data Register

address: VDB base + 8.
attributes: Read 2 wait states, Write 2 wait states.
power up value: undefined.
sizes: 2 kbytes.

bit 0 TTL modulation for Laser 0.
bit 1 TTL modulation for Laser 1.
bit 2 TTL modulation for Laser 2.
bit 3 TTL modulation for Laser 3.

0 = Turn the laser OFF.
1 = Turn the laser ON.

bit 4 Vertical Region Of Interest (VROI).

0 = VROI disable.
1 = VROI enable.

bit 5 Vertical clamping enable.

0 = Clamping disable.
1 = Clamping enable.

bits <7:6> Video channel selection or Vertical interrupt (bit 6).

If the Control Register 0 - Video channel selection mode bit <7:6> = 00 (Mode 0) then the VLUT bits <7:6> control the video channel selection.
00 = Video input channel 0.
01 = Video input channel 1.
10 = Video input channel 2.
11 = Video input channel 3.

If the Control Register 0 - Video channel selection mode bit <7:6> = 10 (Mode 2) then the VLUT bit <7> is not used and the VLUT bit <6> drives the vertical interrupt line (VERT_INTERRUPT) on the Digital Video Bus. Note that the VERT_INTERRUPT rising edge will trigger an interrupt of the CPU of the Digital Processing Board.
X0 = Vertical Interrupt negated.
X1 = Vertical Interrupt asserted.

If the Control Register 0 - Video channel selection mode bit <7:6> = 01 or 11 (Mode 1 or 3) then the VLUT bit <7:6> is not used.
XX =Not used.

See Section 4.1 for more details

2.2 Video Acquisition Mode

Once all the VDB registers are initialized, the VDB is now ready to digitize the analog video signal from the camera and to send the 16-bit pixels at video rate to the DPB.

2.2.1 *The A/D Conversion*

The VDB digitizes the video with a 12-bit analog to digital (A/D) converter and drives the 12-msb of the DATA<15:0> bus. The digital code is in twos complement format. The most negative value corresponds to the minimum video signal amplitude (black) and the most positive value corresponds to the maximum video signal amplitude (white).

If the video amplitude is outside the A/D conversion range, the A/D Converter sets an overflow flag. This flag is routed to the least significant bit DATA0 of the DATA<15:0> bus to inform the DPB of this condition. Also, the overflow is directly flagged to the user by the momentary turning on of a red LED visible from the back of the host computer.

The three lines DATA<3:1> are driven to zero by the VDB. Except for overflow or underflow conditions, the minimum incremental step is 0x0010 or 16 decimal.

Video signal condition	**VIDEO DATA<15:0>**	
	Hexadecimal	**Decimal**
White video signal overflow	0x7FF1	+32 753
Maximum white video signal	0x7FF0	+32 752
Minimum black video signal	0x8000	-32 768
Black video signal underflow	0x8001	-32 767

Digitizing the video signal with a 12-bit A/D in comparison with an 8-bit A/D enables the BIRIS Accelerator System to extract low intensity peaks from the illuminated scene of a laser without the need to vary the video analog gain.

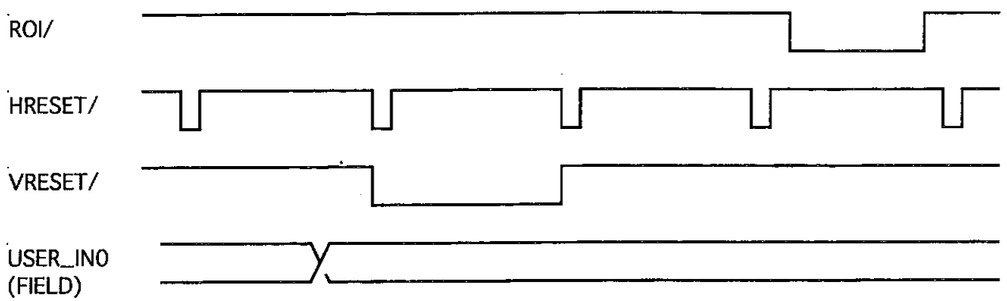
2.2.2 *Timings Related to the Video Bus in Acquisition Mode*

The Digital Video Bus Specifications do not define the exact behavior of all signals. Only general guidelines are provided and the details are left to the design of the specific module. This section will highlight how these issues have been addressed in the implementation of the VDB.

- The signals HRESET/, VRESET/, ROI/, DATA<15:0> and USER_IN0 are all synchronous with the rising edge of PCLK.
- PCLK may not be continuously running. At the end of a video horizontal line, PCLK stops toggling, waits for the next video horizontal SYNC pulse, and then resumes its operation. If the SYNC pulse does not occur, then PCLK remains static.

- For every video horizontal SYNC pulse detected, the HRESET/ is active for a period of one PCLK.
- For every video vertical SYNC pulse detected, the VRESET/ is active for a period of one horizontal line. VRESET/ toggles on the falling edge of HRESET/.
- The video field information will be output on the USER_IN0 line. Its logic level toggles only shortly before the VRESET/ pulse. A logic *zero* indicates the *first* field of a frame, a logic *one* indicates the *second* field.

The next diagram illustrates a few points mentioned above.



3. *The Camera Interface*

The VDB accepts up to four BIRIS sensor video signals but only one is selected at any time. The VDB extracts the synchronization signals from the analog video of the selected sensor. Through software configuration, the VDB accepts standard video formats such as RS170A and CCIR. Nonstandard video signal may be acceptable but will require a specific analysis.

If several BIRIS sensor cameras need to be synchronized, a programmable SYNC generator can provide the signals to slave them together. The Horizontal Drive (HD) and Vertical Drive (VD) available on the connector J11 should be driving the corresponding inputs of all cameras.

With the cameras slaved together it is possible to switch to another camera source and start digitizing its video immediately. Otherwise, switching cameras would require waiting for the beginning of the next video field to start the digitization process.

3.1 The SYNC Generator

The important point about the SYNC Generator is that this device operates independently of the rest of the system. It has its own clock oscillator and synthesizes its output waveforms freely. The device will be used to synthesize the signals required to slave one or several cameras to its timing.

The SYNC Generator is designed around the LM1882 from National Semiconductor. A series of internal registers allows the programming of almost any video timing format. Two of its outputs become, after buffering, the Horizontal Drive and Vertical Drive available on the connector J11.

The SYNC Generator also produces a composite SYNC that can be output onto the connector J11 to synchronize external cameras. Configuring the jumper block J6 allows routing this TTL CSYNC to the SYNC Decoder (Bt261) and locking the video timing to this source, but this mode is not recommended. The camera synchronizes its video timing to an external source with an internal Phase Locked Loop (PLL). This PLL causes the video signal to jitter in reference to the stable CSYNC. Instead of routing CSYNC to the SYNC Decoder (Bt261), it is much better to route the analog video signal and let the Bt261 lock to it.

3.2 The SYNC Decoder

The SYNC Decoder is the brain of the VDB. Designed around the Bt261 from Brooktree, the device extracts the horizontal and vertical syncs from the analog video signal and generates a pixel clock synchronously with the beginning of the video line.

The device operates from an 80 MHz ECL oscillator. This clock is divided down by an internal programmable divider to generate the pixel clock with a minimum jitter.

A list of internal registers must be initialized to conform to the specific video timings expected.

3.3 The LASER Modulation

Since the gain of the analog video input is fixed, it is desirable to have the possibility of varying the emission power of the laser projector. This feature would allow a BIRIS sensor to operate in a larger dynamic range. The laser power reduction would be useful for short range measurements, while increasing the laser power for longer range applications would be helpful.

To comply with this function, the VDB makes available four TTL outputs with individual programmable duty cycles to modulate the laser emission power of each BIRIS sensor. Only one output is active at any time and its selection follows the video input channel selection. The three other outputs are held in an inactive state. The active high or active low polarity of the four signals is fixed with a configuration strap located on the connector J6 pins 7-8 (consult Appendix A for more details).

The modulation waveforms are synthesized from four bits of the Vertical Look-up Table (VLUT). The VLUT is addressed with a counter clocked by the HRESET/ signal and the counter is reset by the VRESET/ pulse. By programming specific patterns into the VLUT one can synthesize virtually any desirable waveforms for the four modulation signals. The only constraint is that the time base for this waveform is one horizontal video line duration. For example, the RS170A video standard horizontal line period is close to 64 µs. So the modulation waveform minimum pulse width would be 64 µs.

With 2 kbytes, the VLUT support video format up to 2048 horizontal lines per frame or 1024 lines per field in interlaced.

4. *VDB Internal Functions*

This section gives important technical details of the internal operation of the VDB design.

4.1 The Video Input Multiplexer

The analog video inputs must be AC coupled since the video DC level of cameras from various manufacturers will be different. A four-to-one video input multiplexer is required to switch dynamically from up to four BIRIS sensors. The Analog Device AD9300 was designed for this function. The device has a unity gain and drives a load of up to 2 kΩ.

The bits<1:0> the of the Control Register 0 or the bits<7:6> of the VLUT drive the digital selection on the video input multiplexer. The bits<7:6> of the Control Register 0 select one of the two possible sources and provide four modes of operation.

Mode	Video Input Channel Selection
0	From VLUT bits <7:6>
1	From CNTRL REG 0 bits <1:0>, with double buffering on VRESET/ falling edge.
2	Same as Mode 1 and the VLUT bit <6> drives the VERT_INTERRUPT of the Digital Video Bus.
3	From CNTRL REG 0 bits <1:0> directly, without double buffering.

Mode 0 Single frame realtime cameras multiplex.

This mode is used when the application requires the processing of several camera signals in a single video time frame. The video input channel selection is directly controlled by the VLUT bits<7:6>. It is then possible to dynamically switch from video sources any time during an active video frame, thus creating a mosaic of images from different cameras in a single video frame. Since the VLUT is clocked from the HRESET/ signals, the channel switching occurs during the video horizontal blanking interval. Note that the cameras must be synchronized.

Mode 1 Video channel selection with double buffering on VRESET/ falling.

This mode is used when the application requires the processing of several camera signals sequentially. The Control Register 0 bits<1:0> select the next video input channel and the channel switching occurs at the end of the current video frame (or field if interlaced video). This mode allows the CPU to update the video input channel selection any time during the video frame.

Mode 2 Same as Mode 1 + Vertical Interrupt enabled.

This mode includes the Mode 1 functionality and the added feature of generating a CPU interrupt on any line during a video frame or field. The VLUT bit<6> is routed to the VERT_INTERRUPT of the Digital Video Bus. The VLUT bit<7> is not used.

Mode 3 Direct video channel selection.

This mode is used when the application requires the processing of a single camera signal. The Control Register 0 bits<1:0> select the video input channel directly, without double buffering. This mode is also required to reset the channel selection in the case of a deadlock condition of the Modes 0, 1, or 2.

Deadlock condition with Modes 0, 1, or 2

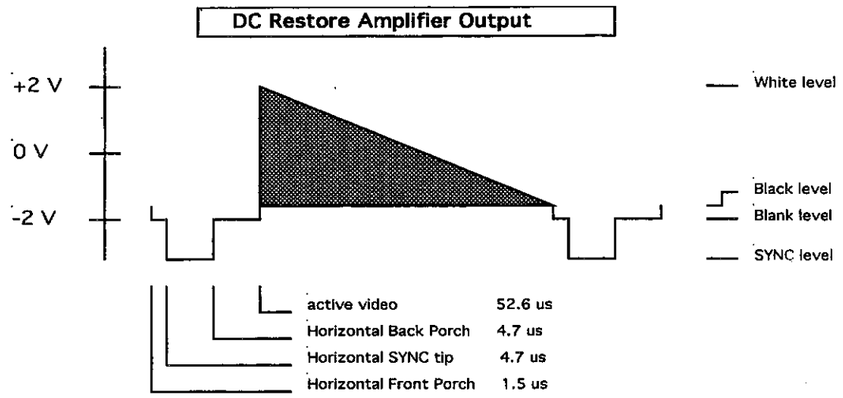
A deadlock condition will occurs for these modes when a video channel is selected and there is no video signal present. To switch from video channels, these modes require the generation of the HRESET and VRESET derived from the sync information of the video signal. If there is no video signal on the actual input selected, neither HRESET nor VRESET is generated and the video channel selection freezes.

The actual video input channel selected can be read from the STATUS register bits<1:0>. The application software will recognize a deadlock condition when reading the STATUS register after a vertical reset (for Mode 1 and 2) or after a specific video line number (for Mode 0) and comparing the actual channel selected with the expected value. In the case of a mismatch, a message should be flagged to the user to indicate the absence of video on this particular channel.

The Mode 3 will get out of this deadlock condition since it bypasses all circuitry and the video input multiplexer is driven directly from the Control Register 0 bits<1:0>.

4.2 The DC Restore Amplifier

Since the video is AC coupled it is desirable to restore the video signal to a fixed DC level before driving the A/D converter. Signal amplification is required as well as the capability of driving a low impedance 150 Ω load. The Elantec EL2090C part was chosen.



The clamping pulse will be asserted for 3 µs in the middle of the horizontal back porch and will clamp the video to the −2.0 V DC level.

A −2 V voltage reference designed from a combination of a 6.2 V zener diode and a few resistors is adequate since the reference is required for only a short period of time and its noise figure is not critical.

The amplifier gain should be such that a 0.7 V video input produces a ±2 V swing at the output. The output signal will be attenuated by two before reaching the inputs of the A/D converter with a full ±1 V swing.

Note that only the video signal that will be digitized needs to be limited to the ±1 V range of the A/D inputs. The video sync tip level will reach −1.9 V and the A/D inputs are designed to recover from such an under voltage.

4.3 The Low Pass Filter

A linear phase passive 2.0 MHz low pass filter with and 100 Ω impedance filters the video signal from the DC Restore amplifier to the inputs of the A/D Converter.

4.4 The Analog to Digital Converter

The Analog Device AD872 converts the ±1 V video signal feed at its inputs to a 12-bit digital code in twos complement format. The device will be operated at up to 10×10^6 samples/second.

4.5 The SYNC decoder and Pixel Clock Synchronizer

The ZERO output is used for the Horizontal Region Of Interest (HROI) generation. The HSYNC and VSYNC outputs are used to synthesize the HRESET and VRESET signals.

4.6 The Vertical Look-up Table (VLUT)

The VLUT is a 2K × 8-bit static RAM used for the generation of several signal waveforms that are important to the video acquisition process. While acquiring video, the VLUT address is provided by a 10-bit binary counter and the most significant address bit is driven by the FIELD signal. The VLUT address is reset to zero at the beginning of the first video field or is preset to 1024 at the beginning of the second video field in interlaced acquisition. The address is then incremented by one count at the beginning of each horizontal video line. In summary

- the address counter resets on each VRESET/ pulse
- the address counter increments by one count on each HRESET/ pulse
- the FIELD signal drives the most significant address bit of the VLUT.

This hardware resource allows the generation of signals to be controlled on a video line-by-line basis and can discriminates a specific field in interlaced video. The VDB design uses the VLUT to synthesize these signals:

- The four TTL modulation signals needed to control the power emission of the laser.
- The Vertical Region Of Interest (VROI) to start and stop the pixel processing on specific video lines.

- The vertical clamping enables the DC restore outside the vertical sync interval.
- The video input channel selection.

The VDB design uses four bits from the VLUT to synthesize the modulation signals of the four laser. Patterns of four independent waveforms can be programmed and the modulation may be enable synchronously with the video timing.

The VROI would normally be programmed to start before the first displayed line of the field 0 and stop before the last one to skip the last half displayed line of the interlaced format. It would start with the second displayed line of the field 1 to skip the first half line and stop after the last displayed line of field one.

The DC restore circuitry clamps the video signal during the horizontal back porch. At this time the video is at the blank level, just before the start of the displayed line. Throughout the vertical sync interval, the DC restore should be disabled to prevent the clamping of the video at the sync tip level. Otherwise, a large error signal would shift the video DC level and it would take several video lines to recover from this step change.

4.6.1 *Programming the Vertical Look-up Table*

In programming mode the VLUT is addressed with a 11-bit binary counter incremented after each register read or write cycle. The address counter cannot preset to a random value, it can only reset to zero. So the complete 2048 registers must be initialized sequentially.

The following programming algorithm must be followed:

1. Control Register 0 bits <5:4> = 11. This puts the address counter in programming mode and resets it to zero.
2. Control Register 0 bit 5 = 0. This removes the reset condition and allows the address counter to increment after each register read or write cycle to the VLUT.
3. Fill the VLUT with 2048 write cycles to the VLUT Data Register.
4. Control Register 0 bit 5 = 1. This resets the address counter to zero.
5. Control Register 0 bit 5 = 0. This removes the reset condition and allows the address counter to increment after each register read or write cycle to the VLUT.
6. Read back the 2048 entries from the VLUT Data Register for verification.
7. Control Register 0 bit 5 = 1. This resets the address counter to zero.
8. Control Register 0 bits <5:4> = 00. This puts the address counter into video acquisition mode and allows it to increment on each HRESET/ pulse.

Note that steps 5, 6, and 7 are to be performed only if a read back verification is required.

5. *Electrical and Mechanical Specifications*

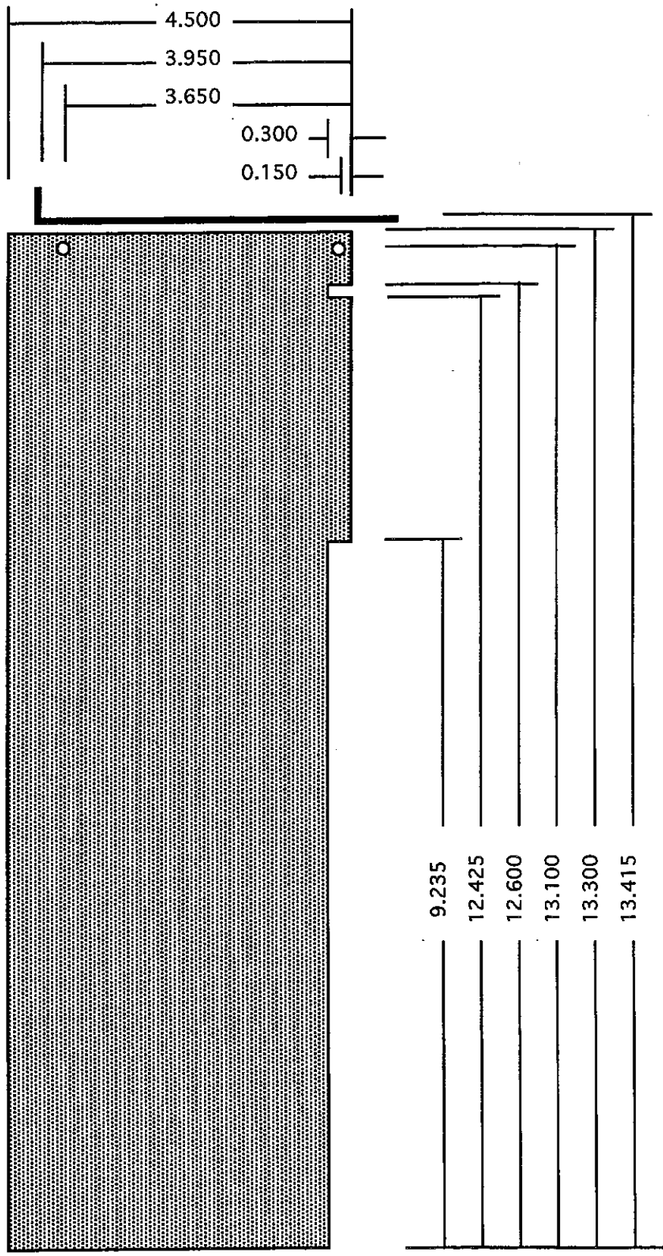
The VDB is a full-sized PC/AT board occupying a single 8-bit expansion slot in the host computer chassis. Since all registers are programmed through the Digital Video Bus, there is no need for a PC/AT bus interface on this board and, thus, the VDB requires only the power supplies from its host computer.

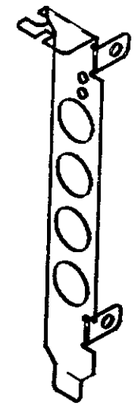
5.1 Electrical Specifications

5.1.1 *VDB Power Supply Requirements*

Supply (Volts)	**Current (Amp)**		**Power (Watts)**	
	Typical	Maximum	Typical	Maximum
+ 5	2.72	5.47	13.6	27.4
+ 12	0.10	0.15	1.20	1.80
- 12	0.15	0.20	1.80	2.40

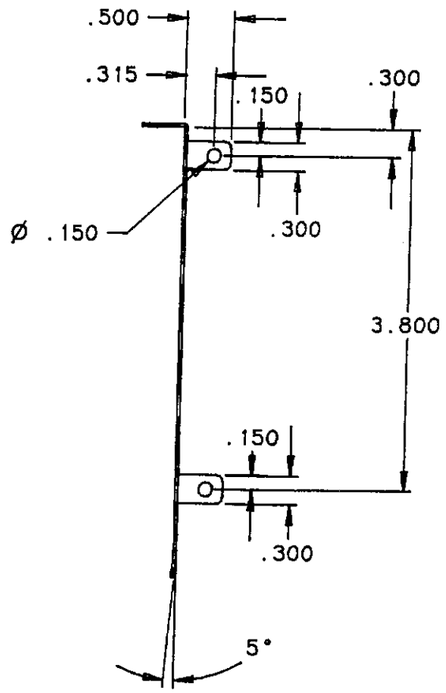
5.2 Mechanical Specifications

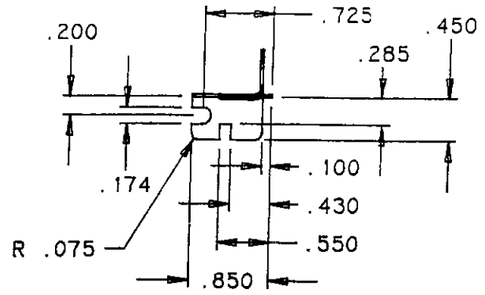


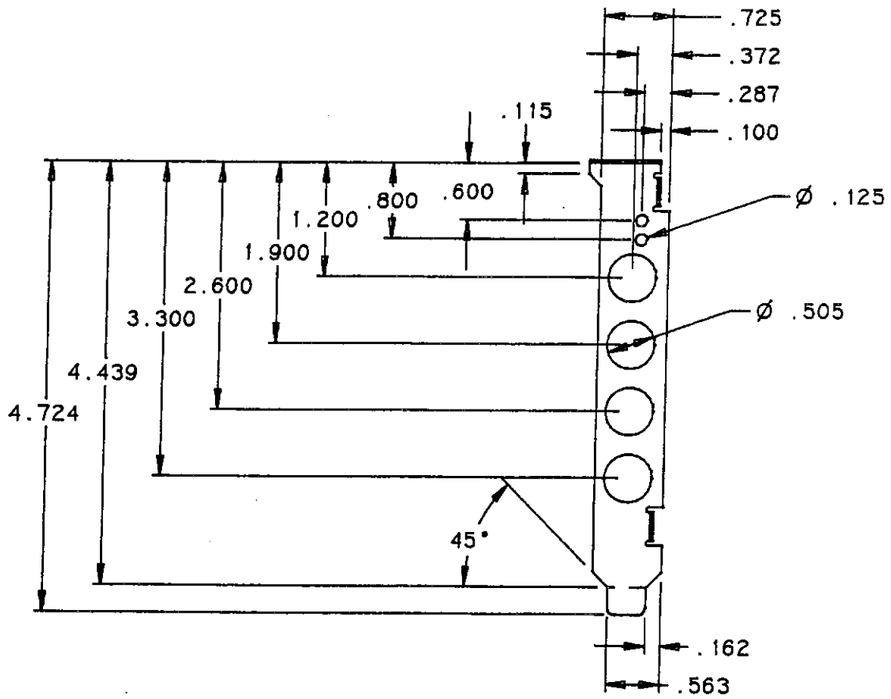


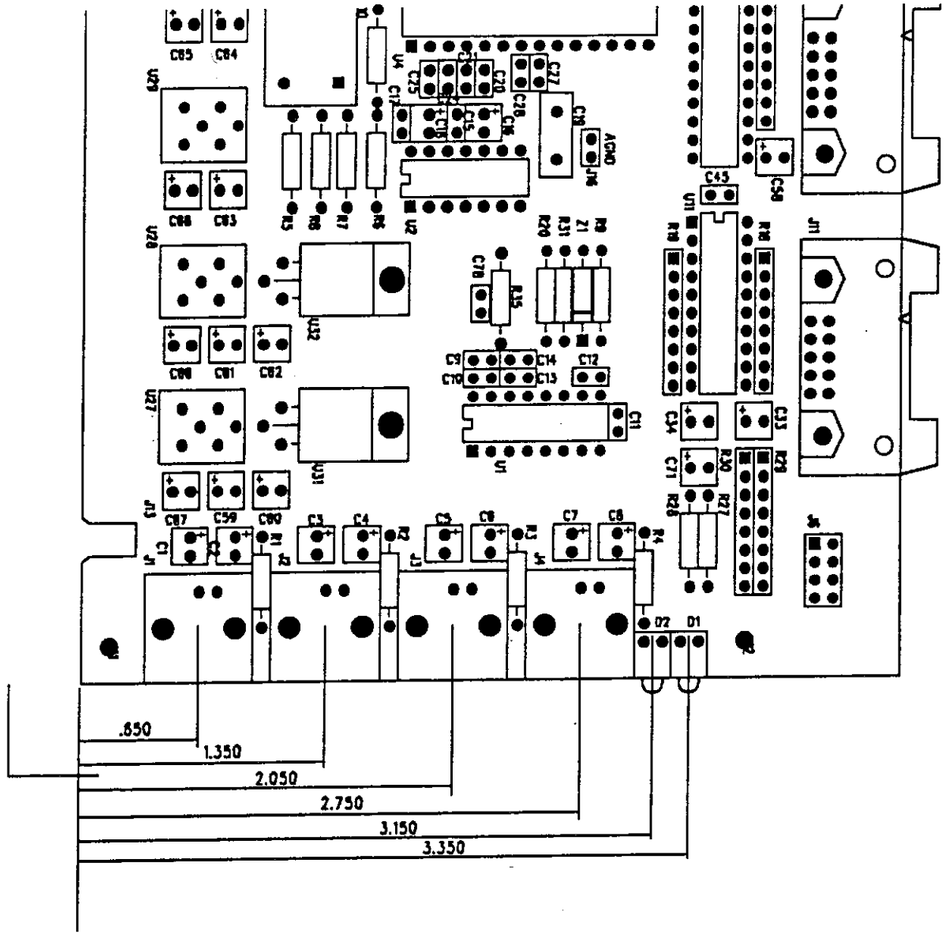
BIRIS Accelerator
PC Card Mount

Material: .030 Steel
File: C:\MECH\BIRIS\ACCEL\pc_mount
D. Taylor June 9, 1994




.200
.725
.450
.285
.174
.100
.430
R .075
.550
.850

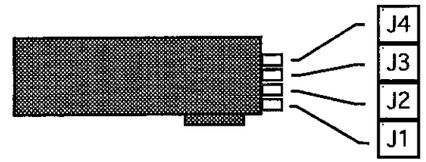

.725
.372
.287
.115
.100
.800
.600
1.200
Ø .125
1.900
2.600
3.300
Ø .505
4.439
4.724
45°
.162
.563


.650
1.350
2.050
2.750
3.150
3.350

Appendix A. VDB Configuration Jumper Blocks and Connectors

A1. J1 to J4: Analog Video Inputs BNC Connectors

J1 to J4 are four BNC socket connectors. They are accessible at the rear panel of the computer when the PCB is inserted into the PC/AT expansion slot.

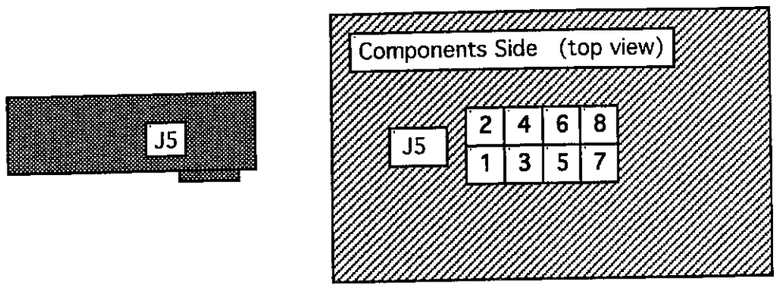


Connector	Description
J1	Analog video input channel 0 (selected by default).
J2	Analog video input channel 1.
J3	Analog video input channel 2.
J4	Analog video input channel 3.

Each input is AC-coupled and terminated with a 75 Ω load. The four analog inputs are routed to the video input multiplexer. The application software selects the channel 0 from J1 as the default video input.

A2. J5: SYNC Decoder Input Select Configuration Jumpers Block

J5 is an 8-pin configuration jumper block. It is located near the center of the VDB PCB. It is not accessible when the PCB is inserted into the PC/AT expansion slot.

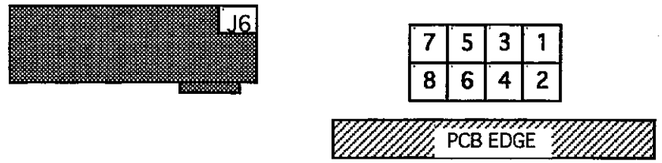


J5 selects one of the three SYNC sources and routes it to the SYNC Decoder. The three possible SYNC sources are the external Analog or TTL composite SYNC or the VIDEO signal output from the 4:1 multiplexer.

Jumpers Positions	Description
1 - 2 strap in:	75 Ω input impedance. May be required if the Analog CSYNC is selected.
strap out (default):	High input impedance.
3 - 4 strap in:	Analog CSYNC (from J11 pin 10) input to the SYNC decoder.
strap out (default):	Analog CSYNC not used.
5 - 6 strap in:	TTL CSYNC (from J11 pin 6) input to SYNC decoder.
strap out (default):	TTL CSYNC not used.
7 - 8 strap in (default):	Analog VIDEO signal input to the SYNC decoder.
strap out:	Analog VIDEO signal not used.

A3. J6: CSYNC IN/OUT, Pixel Clock IN/OUT, LASER Modulation Polarity Configuration Jumpers Block

J6 is an 8-pin right angle configuration jumper block. It is located near the top right-hand corner of the VDB PCB. It is accessible even when the PCB is inserted into the PC/AT expansion slot.

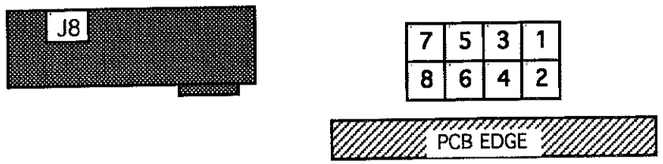


Jumpers Positions	Description
1 - 3 strap in:	TTL CSYNC inputs from J11 pin 8.
3 - 5 strap in (default):	TTL CSYNC outputs on J11 pin 8.
2 - 4 strap in:	TTL CLOCK inputs from J11 pin 2.
4 - 6 strap in (default):	TTL CLOCK outputs on J11 pin 2.
7 - 8 strap in (default):	LASER Power TTL Modulation is active low. A logic 0 turns the laser power ON, a logic 1 turns it OFF.
strap out:	LASER Power TTL Modulation is active high. A logic 0 turns the laser power OFF, a logic 1 turns it ON.

A4. J8: VDB Register Base Address Configuration Jumpers Block

J8 is an 8-pin right angle configuration jumper block. It is located near the top left-hand corner of the VDB PCB. It is accessible even when the PCB is inserted into the PC/AT expansion slot.

The Video Bus Register address space is limited to 256 registers (8-bit address bus). The VDB reserves 16 of those locations for on board registers mapping. So the VDB decodes the 4-lsb of the address bus for its registers while the 4-msb are used for multiple boards selection.



Jumpers Positions	Description	Straps	
1 - 2	Base Address 0 (lsb)	strap in (default) = 0,	strap out = 1
3 - 4	Base Address 1	strap in (default) = 0,	strap out = 1
5 - 6	Base Address 2	strap in (default) = 0,	strap out = 1
7 - 8	Base Address 3 (msb)	strap in (default) = 0,	strap out = 1

The four straps are installed with the default configuration and the VDB registers are mapped at the base address of 0x00.

A5. J10: Video Bus Connector

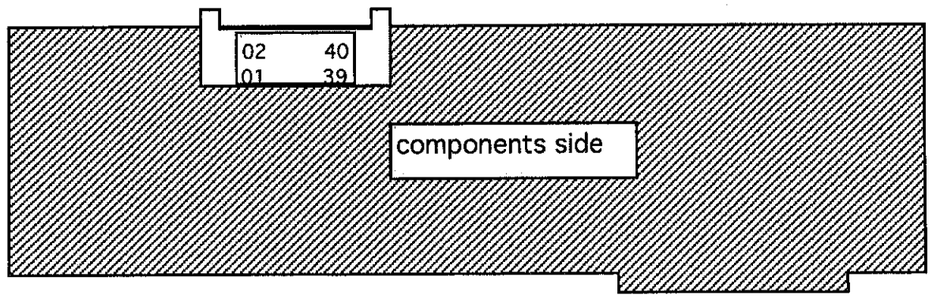
The VDB board is connected to the Video Bus with a 40-pin right angle header located on the top of the board.

Mechanical clearance must be accounted for the female socket when positioning the male header onto the top of the PCB. The VDB uses a 0.300 in. clearance.

Right Angle Header Pinout

View from the components side:

GND	---- 01	02 ----	REGCLK
GND	---- 03	04 ----	BUSCNTRL0
DS/	---- 05	06 ----	BUSCNTRL1
DTACK/	---- 07	08 ----	GND
DATA00	---- 09	10 ----	DATA01
DATA02	----11	12 ----	DATA03
GND	----13	14 ----	DATA05
DATA04	----15	16 ----	DATA07
DATA06	----17	18 ----	GND
DATA08	---- 19	20 ----	DATA09
DATA1	---- 21	22 ----	DATA11
GND	---- 23	24 ----	DATA13
VDATA12	---- 25	26 ----	DATA15
VDATA14	---- 27	28 ----	GND
SPARE0	---- 29	30 ----	USER_IN0 (FIELD ID)
SPARE1	---- 31	32 ----	USER_IN1
ROI/	---- 33	34 ----	USER_OUT0
VRESET/	---- 35	36 ----	USER_OUT1
HRESET/	---- 37	38 ----	GND
PCLK	---- 39	40 ----	GND



A6. J11: Camera Synchronization Signals Connector

J11 is a 10-pin right angle connector located near the top right-hand corner of the VDB PCB. Five camera synchronization signals are available as inputs or outputs.

Right Angle Header Pinout

View from the components side:

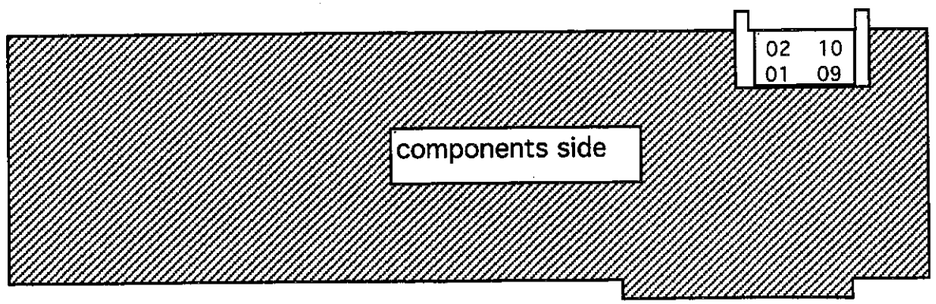
GND ---- 01	02 ---- EXT. CLOCK	(input or output)
GND ---- 03	04 ---- HORIZONTAL DRIVE	(output)
GND ---- 05	06 ---- VERTICAL DRIVE	(output)
GND ---- 07	08 ---- TTL CSYNC	(input or output)
GND ---- 09	10 ---- ANALOG CSYNC	(input)

EXT. CLOCK:
With a maximum frequency of 10 Mhz this TTL signal can be an input or an output depending on the strapping of the configuration block J6.

HORIZONTAL and VERTICAL DRIVES:
These TTL outputs are used to slave the video timing of one or several cameras. Their timings are fully programmable. The default software configuration drives RS170A cameras.

TTL CSYNC:
This TTL Composite SYNC signal can be an input or an output.

ANALOG CSYNC:
This analog input is AC-coupled and can be terminated by a 75 Ω load (configuration jumper block J5, pins 1-2). A 1 V p-p maximum signal amplitude is expected.



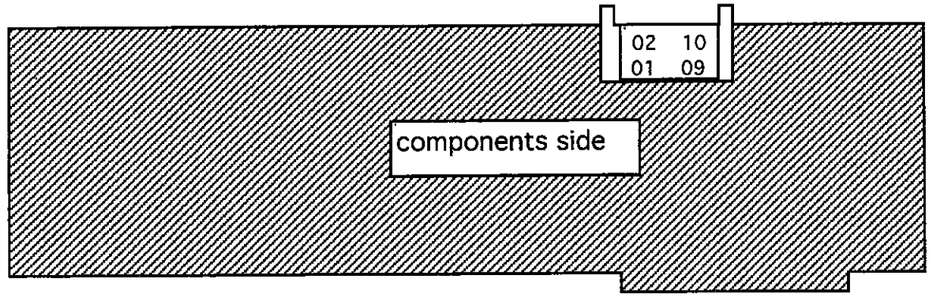
A7. J12: Laser Output Power Modulation Signals Connector

J12 is a 10-pin right angle connector located near the top right-hand corner of the VDB PCB. Four TTL output signals with individual programmable duty cycles can modulate the emission power of up to four laser projectors. The signal polarity (active high or low) of the four TTL outputs is selected with the configuration jumper block J6 pins 7-8. Only one output will be modulated at any time, the other three will be inactive high or low depending on J6 pins 7-8. The selection of the active laser modulation channel follows the camera channel selection through software control.

Right Angle Header Pinout

View from the components side:

GND ---- 01	02 ---- TTL MODULATION LASER 0
GND ---- 03	04 ---- TTL MODULATION LASER 1
GND ---- 05	06 ---- TTL MODULATION LASER 2
GND ---- 07	08 ---- TTL MODULATION LASER 3
GND ---- 09	10 ---- +12 V @ 1.3 Amp. max. (from PC/AT supply)



A8. Indicator RED and GREEN LEDs

One red and one green indicator LED is visible from the PC/AT rear panel when the VDB board is installed into one of the PC/AT expansion slots.

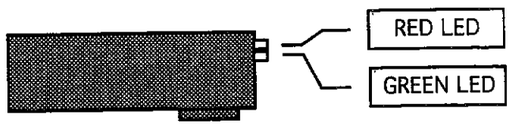
During the power-up, both LEDs should flash momentarily for 0.25 s. After the power-up sequence, the green LED should stay ON while the red LED should be OFF.

GREEN LED: VDB Register Access.

The green LED monitors on board register access cycles. At any time a register is accessed via the Digital Video Bus by the DPB board, the green LED flashes OFF for 0.25 s.

RED LED: A/D Overflow.

The red LED flashes ON for 0.25 s when the video input of the A/D converter is out of the ±1.0 V range. The A/D overflow is only signalled during the active processing window (Region Of Interest or ROI). Outside the ROI, the trigger is disabled to prevent undesirable A/D overflows cause by the DC restore circuit during the horizontal and vertical video blanking.



Appendix B. Parts Ordering Instructions

All resistors must be metal film, 1/4 W, 1% tolerance. Only R27 and R28 470 Ω resistors may be of carbon type with 10% tolerance (they are used for the LEDs D1 and D2).

Things that are not listed in the Bill Of Material (BOM):

(1) Metal bracket for the PCB (custom built).
(2) Heat sinks for the TO-220s (FUTURE ELECTRONICS Inc. P/N 5771B).

(4) Screws and nuts for the two heat sinks and for the metal bracket.
6-32 × 1/4 in. steel plated binding head screw.
6-32 hexagon nuts (small diameter, SPAE-NAUR No B-1521, or NRC Store No 470-10-001-115) are required.

7.5 in. of 40 conductor ribbon flat cable (from Electro Sonic Inc. P/N 3365-40).
(2) 40 pin female crimp connectors (from Electro Sonic Inc. P/N 3417-660).

(9) Configuration straps (jumpers, from Samtec Inc. P/N SNT-100-BK-G).

Flux residue remover.
Heat conducting grease.

(1) 5 m, 75 Ω coaxial video cable

Appendix C. PCB Assembly Instructions

Assemble boards only on a static protected bench and wear an anti-static wrist strap.

Assemble the A/D converter U4 last ($300.00 each part and static sensitive).

All the PALs should be mounted on IC sockets:

4 × 20 pins DIP sockets for U9, U20, U25, U36.

2 × 24 pins DIP sockets for U17, U19.

The Brooktree Bt-261 U8 must be mounted on a 28-pin PLCC socket (solder tail socket, not surface mount).

Note that the footprint of the location U3 is voluntarily inverted. The pin 1 (with a square pad) is in the top right-hand position. The part to be installed in U3 is a low pass filter packaged in a 4-pin case with the pin 1 identified with the label "IN". So install the device into location U3 with the pin label "IN" in the top right-hand position of the location.

Install a 74ALS520 or a 74ALS521 in the U15 location. Both parts are compatible for this design.

R32 (100 Ω), R33 (390 Ω), and R34 (390 Ω) are ECL terminating and pull down resistors for the OSC2 80 MHz ECL oscillator. They must not be installed since the oscillators bought from M-TRON have them built in.

C51 (0.1 µF) and C57 (0.1 µF) capacitors are not required since they are used as supply decoupling for the two spare IC locations U18 and U24.

Install a 0.025 in. straight pin connector into location J14. Short the two pins with a strap.

J7, 9, 15, and 16 are hooks of the test probes. The hooks are made by bending a #20 gauge wire in a U shape.

The two TO-220 voltage regulators U31 and U32 must be mounted on heat sinks. Two 1/4 in. 6-32 plated steel binding head screw with two 6-32 hexagon nuts (small diameter, SPAE-NAUR No B-1521, or NRC Store No 470-10-001-115) are required. A thin coating of heat conducting grease should be applied between the heat sinks and the TO-220 packages.

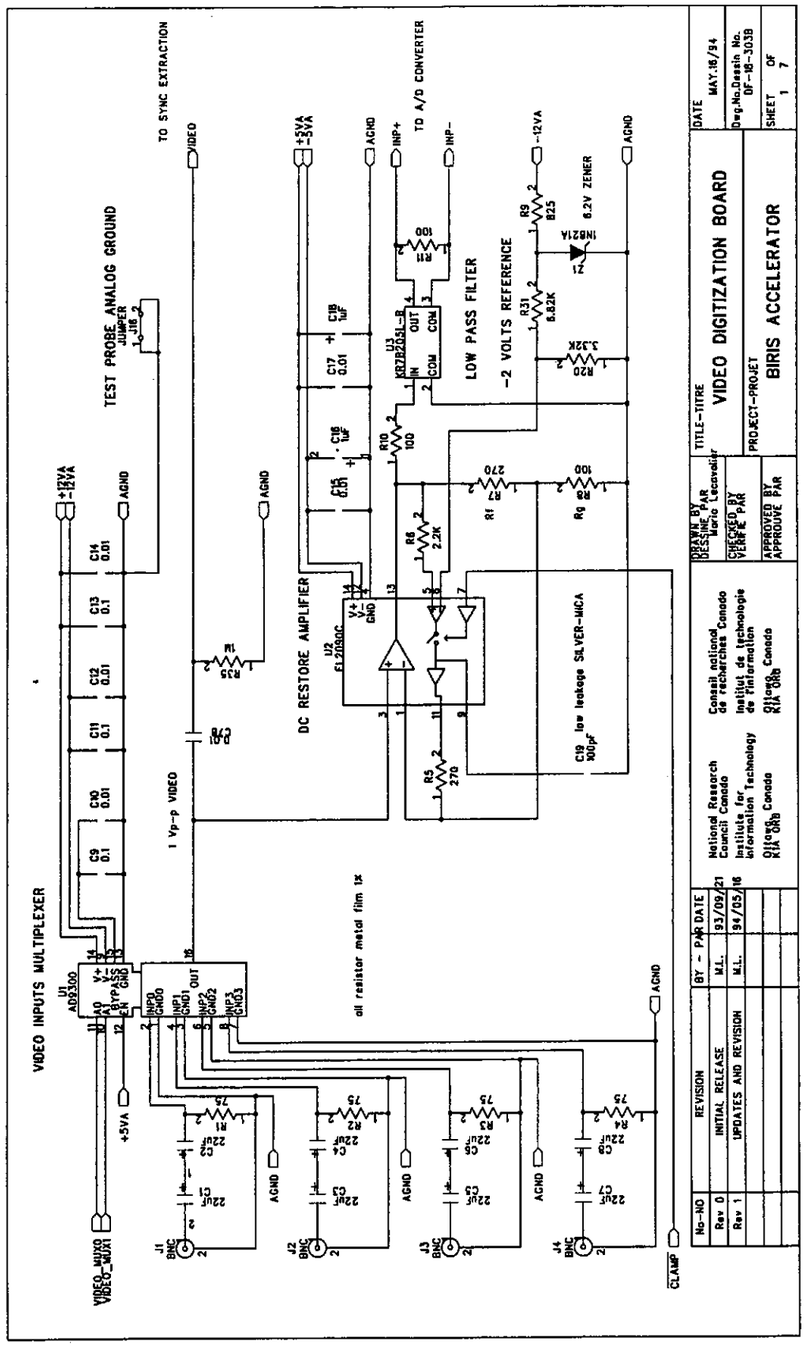
The metal bracket will be secured to the PCB with two 1/4 in. 6-32 plated steel binding head screw and two 6-32 hexagon nuts.

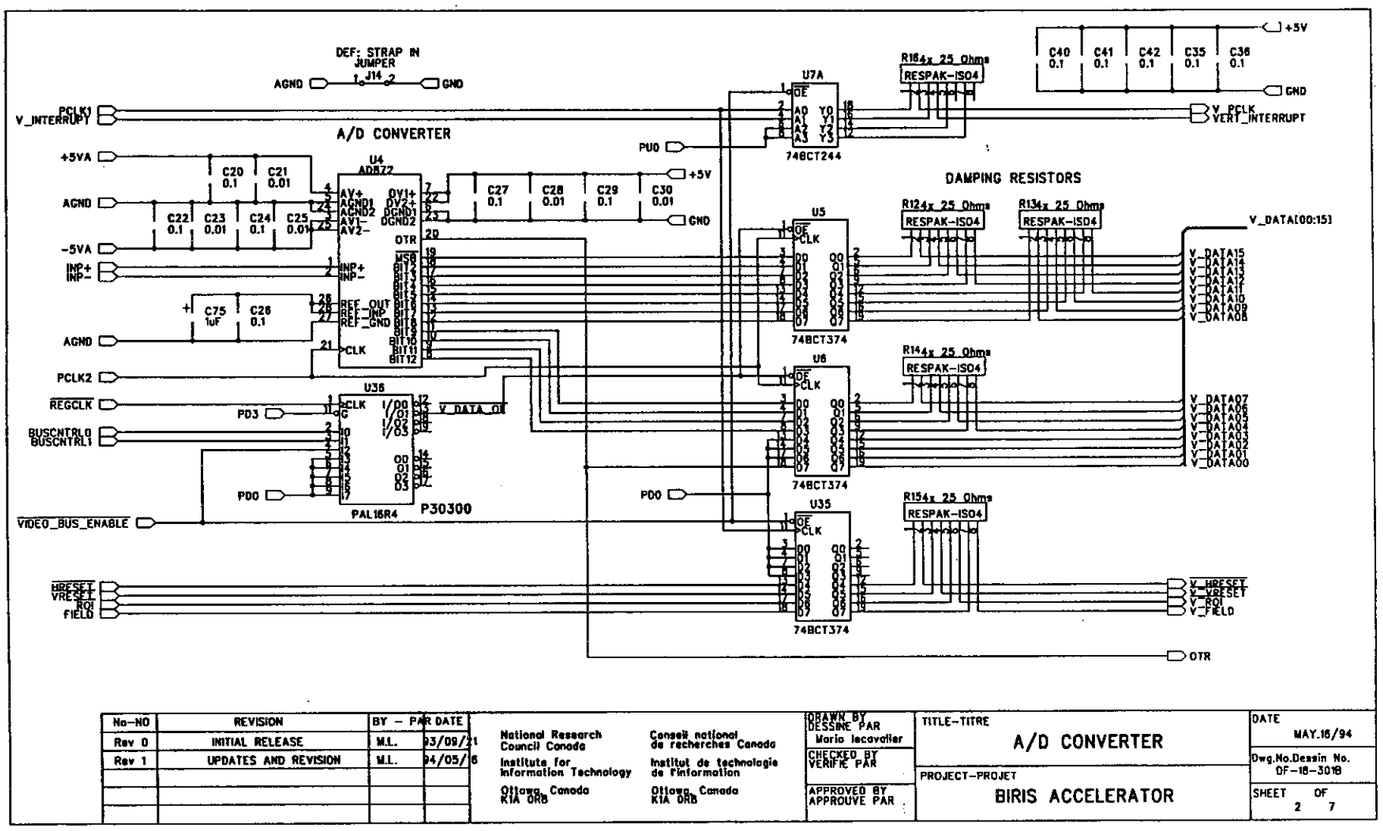
Crimp the two 40 pin female connectors to the 7.5 in. 40 conductor ribbon flat cable.

Appendix D. VDB Test Procedure

No formal software test was ever written to diagnose hardware faults of the Video Digitization Board. It will be up to the licensee of the BIRIS technology to create such tools if he requires them.

Appendix E. VDB Electrical Schematics



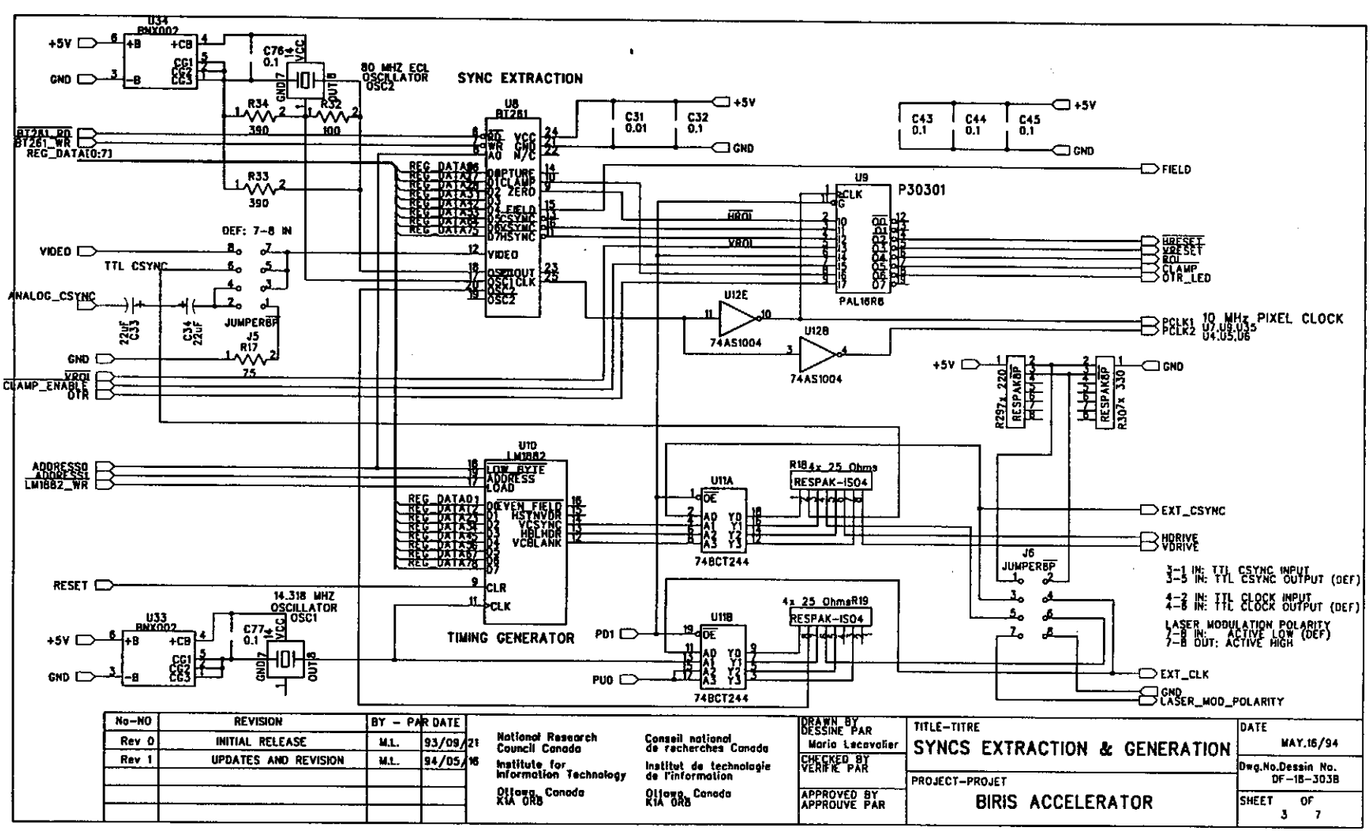


No-NO	REVISION	BY - PAR	DATE
Rev 0	INITIAL RELEASE	M.L.	93/09/21
Rev 1	UPDATES AND REVISION	M.L.	94/05/16

National Research Council Canada / Conseil national de recherches Canada
Institute for Information Technology / Institut de technologie de l'information
Ottawa, Canada K1A 0R6 / Ottawa, Canada K1A 0R6

DRAWN BY / DESSINE PAR: Mario Lecavalier
CHECKED BY / VERIFIE PAR:
APPROVED BY / APPROUVE PAR:

TITLE-TITRE: A/D CONVERTER
PROJECT-PROJET: BIRIS ACCELERATOR
DATE: MAY.16/94
Dwg.No.Dessin No.: DF-18-3018
SHEET 2 OF 7

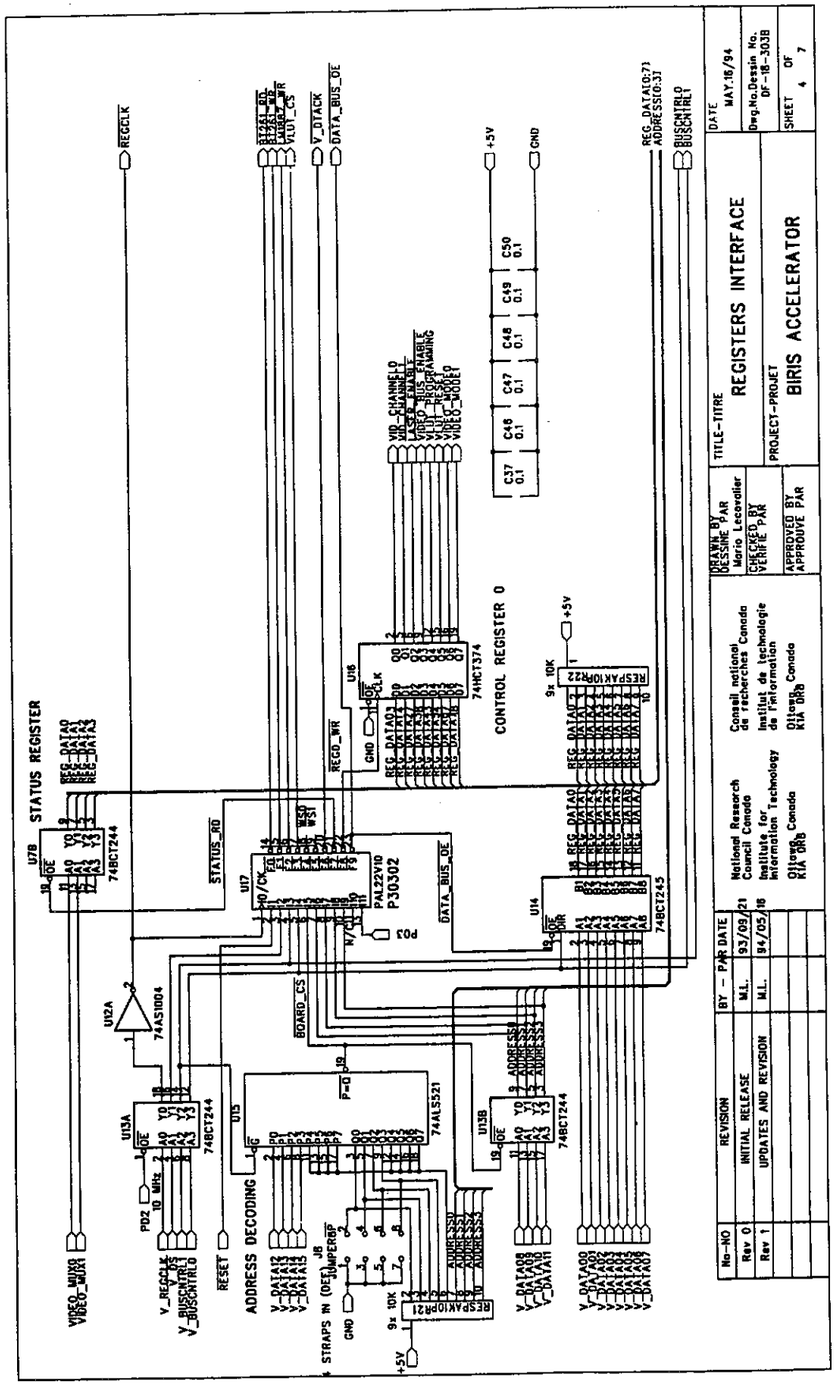


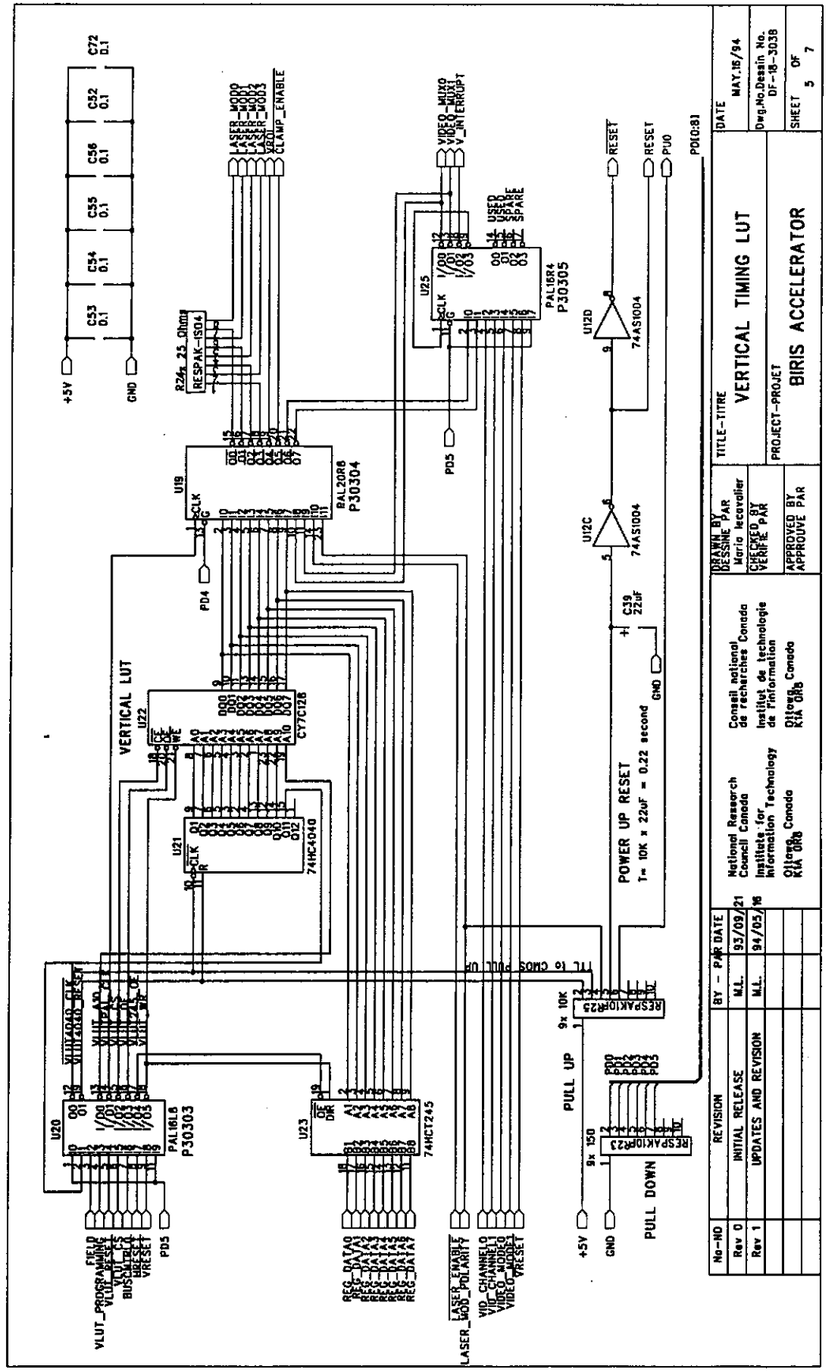
No-NO	REVISION	BY - PAR	DATE
Rev 0	INITIAL RELEASE	M.L.	93/09/21
Rev 1	UPDATES AND REVISION	M.L.	94/05/16

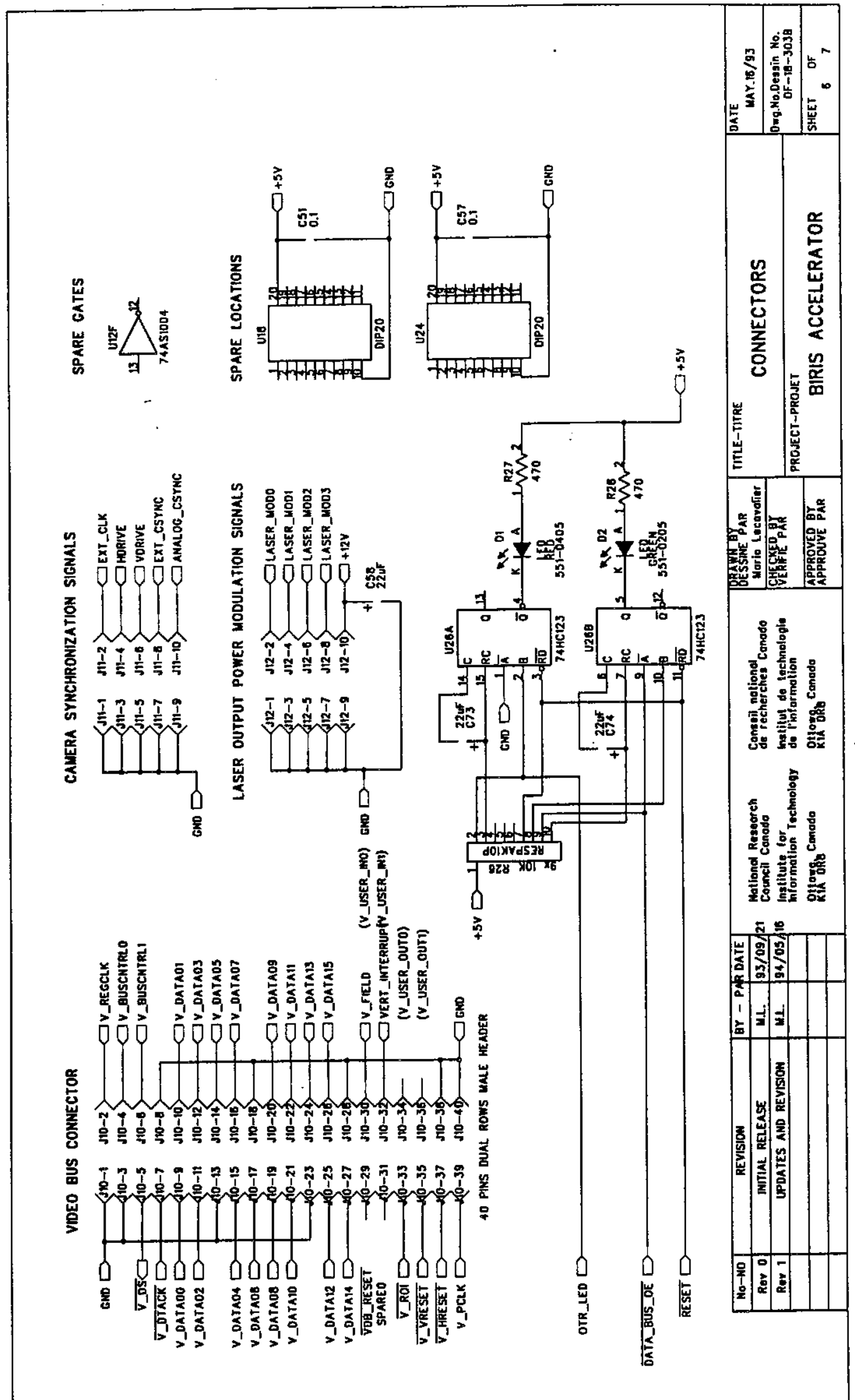
National Research Council Canada / Conseil national de recherches Canada
Institute for Information Technology / Institut de technologie de l'information
Ottawa, Canada K1A 0R6 / Ottawa, Canada K1A 0R6

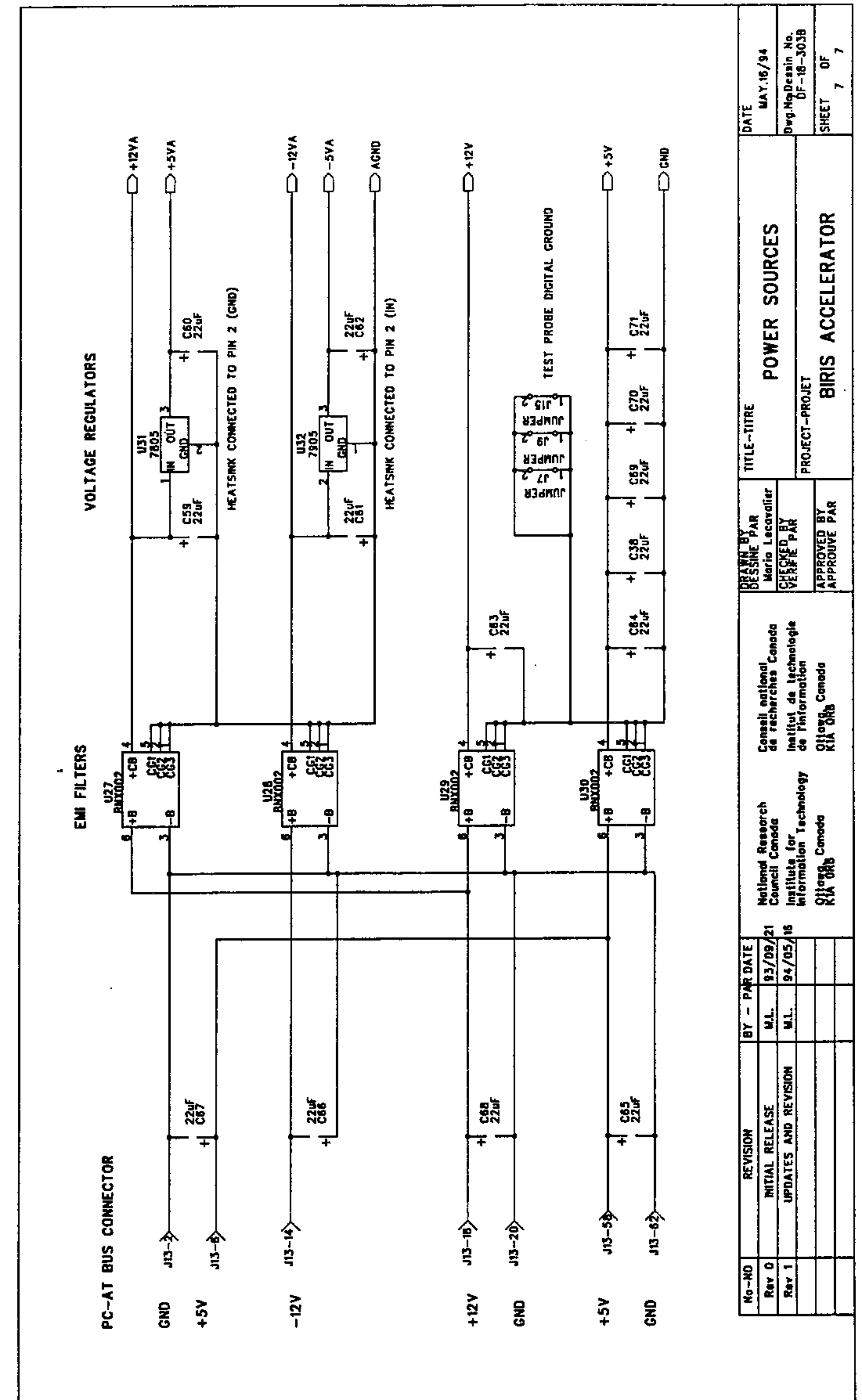
DRAWN BY / DESSINE PAR: Mario Lecavalier
CHECKED BY / VERIFIE PAR:
APPROVED BY / APPROUVE PAR:

TITLE-TITRE: SYNCS EXTRACTION & GENERATION
PROJECT-PROJET: BIRIS ACCELERATOR
DATE: MAY.16/94
Dwg.No.Dessin No.: DF-18-3038
SHEET 3 OF 7


REGCLK
VIDEO_MUX0
VIDEO_MUX1
V_DTACK
DATA_BUS_OE
VLUT_CS
VIDEO_MODE0
VIDEO_MODE1
VLUT_PROGRAMMING
VIDEO_BUS_ENABLE
VIDEO_MODE2
VIDEO_MODE3
+5V
GND
C57 0.1
C46 0.1
C47 0.1
C48 0.1
C49 0.1
C50 0.1
REG_DATA10:7
ADDRESS10:3
BUSCNTRL0
BUSCNTRL1
STATUS REGISTER
CONTROL REGISTER 0
ADDRESS DECODING
STRAPS IN (DEF) JUMPERS
PULL UP
PULL DOWN
REGISTERS INTERFACE
BIRIS ACCELERATOR
DATE MAY.16/94
SHEET 4 OF 7
Dwg.No.Desein No. DF-18-3038
DRAWN BY / DESSINE PAR Mario Lecavalier
CHECKED BY / VERIFIE PAR
APPROVED BY / APPROUVE PAR
National Research Council Canada
Institute for Information Technology
Conseil national de recherches Canada
Institut de technologie de l'information
Ottawa, Canada K1A 0R6
No-NO | REVISION | BY | DATE
Rev 0 | INITIAL RELEASE | M.L. | 93/09/21
Rev 1 | UPDATES AND REVISION | M.L. | 94/05/16


C53 0.1
C54 0.1
C55 0.1
C56 0.1
C52 0.1
C72 0.1
+5V
GND
LASER_MOD0
LASER_MOD1
LASER_MOD2
LASER_MOD3
VCO1
CLAMP_ENABLE
VIDEO_MUX0
VIDEO_MUX1
V_INTERRUPT
RESET
PU0
PD0:3
PD4
PD5
U19
U25
U12C
U12D
74AS1004
PAL16R4 P30305
BAL20R6 P30304
PAL16L6 P30303
VERTICAL LUT
CY7C128
74HC4040
74HCT245
POWER UP RESET
T= 10K x 22uF = 0.22 second
PULL UP
PULL DOWN
VERTICAL TIMING LUT
BIRIS ACCELERATOR
DATE MAY.16/94
SHEET 5 OF 7
Dwg.No.Desein No. DF-18-3038
DRAWN BY / DESSINE PAR Mario Lecavalier
CHECKED BY / VERIFIE PAR
APPROVED BY / APPROUVE PAR
National Research Council Canada
Institute for Information Technology
Conseil national de recherches Canada
Institut de technologie de l'information
Ottawa, Canada K1A 0R6
No-NO | REVISION | BY | DATE
Rev 0 | INITIAL RELEASE | M.L. | 93/09/21
Rev 1 | UPDATES AND REVISION | M.L. | 94/05/16


VIDEO BUS CONNECTOR
CAMERA SYNCHRONIZATION SIGNALS
LASER OUTPUT POWER MODULATION SIGNALS
SPARE GATES
SPARE LOCATIONS
CONNECTORS
BIRIS ACCELERATOR


PC-AT BUS CONNECTOR
EMI FILTERS
VOLTAGE REGULATORS
POWER SOURCES
BIRIS ACCELERATOR

07/05/1994 10:44 Filename: BOM.LST Page 2

28	1	Z1	DIODE-ZENER		STATIC RAM
27	2	U18 U24	DIP20		3V Lithium ZENER
					GENERIC 20 PIN DUAL INLINE
26	1	U2	EL2090C		PACKAGE (DIP) PCB DECAL
					100 MHz DC-RESTORED VIDEO
29	5	J7 J9	JUMPER		AMPLIFIER, 14 PIN DIP
		J14-16			
30	3	J5-6 J8	JUMPER\8P		4 PIN X 2 ROW 0.100 JUMPER
					BLOCKS
31	1	U3	KR78Z05L-8		
32	2	D1-2	LED		LIGHT EMITTING DIODE
33	1	U10	LM1882		PROGRAMMABLE VIDEO SYNC
					GENERATOR, 20 PIN DIP
34	1	OSC1	OSCILLATOR,		
			14.318 MHZ		
35	1	OSC2	OSCILLATOR,80		
			MHZ ECL		
36	1	U20	PAL16L8		PROGRAMMABLE ARRAY LOGIC
					(PAL)
37	2	U25 U36	PAL16R4		PROGRAMMABLE ARRAY LOGIC
					(PAL)
38	1	U9	PAL16R8		PROGRAMMABLE ARRAY LOGIC
					(PAL)
39	1	U19	PAL20R8		PROGRAMMABLE ARRAY LOGIC
					(PAL)
40	1	U17	PAL22V10		EPROM Programmable Array
					Logic (PAL) ELEM
41	4	R8 R10-11	R1/4W,100		RES BODY:100 CENTERS:500
		R32			
42	1	R35	R1/4W,1K		RES BODY:100 CENTERS:500
43	1	R6	R1/4W,2.7K		RES BODY:100 CENTERS:500
44	2	R5 R7	R1/4W,3.32K		RES BODY:100 CENTERS:500
45	2	R20	R1/4W,330		RES BODY:100 CENTERS:500
46	2	R33-34	R1/4W,470		RES BODY:100 CENTERS:500
47	2	R27-28	R1/4W,6.82K		RES BODY:100 CENTERS:500
48	1	R31	R1/4W,75		RES BODY:100 CENTERS:500
49	5	R1-4 R17	R1/4W,825		RES BODY:100 CENTERS:500
50	1	R9	RESPAK-1304,4x		RESISTOR NETWORK, 4
51	8	R12-16	25 Ohms,5%		ISOLATED RES., 8 PIN SIP
		R18-19			0.100
		R24			
52	4	R21-22	RESPAK10P,8x		RESISTOR NETWORK, 9
		R25-26	10K,5%		CONNECTED RES, 10 PIN SIP
					0.100
53	1	R23	RESPAK10P,8x		RESISTOR NETWORK, 9
			150,5%		CONNECTED RES, 10 PIN SIP
					0.100
54	1	R29	RESPAK18P,7x		7 RESISTORS, 1 COMMON, SIP
			220,5%		8 PIN, 0.100 CENTERS
55	1	R30	RESPAK18P,7x		7 RESISTORS, 1 COMMON, SIP
			330,5%		8 PIN, 0.100 CENTERS

07/05/1994 10:44 Filename: BOM.LST Page 1

Bill Of Materials for DF18-303.SCH on Tue Jul 05 10:44:40 1994

Item	Qty	Reference	Part Name	Manufacturer	Description
1	1	U31	7805,.2%		+5 VOLTS REGULATOR, 1.5 AMPS, TO-220
2	1	U32	7905,.2%		-5 VOLTS REGULATOR, 1.5 AMPS, TO-220
3	1	U15	74ALS521		8-BIT IDENTITY COMPARATOR
4	1	U12	74AS1004		HEX INVERTING DRIVER
5	3	U7 U11	74BCT244		OCTAL BUFFER/LINE DRIVER 3
		U13			STATE OUTPUTS
6	1	U14	74BCT245		OCTAL BUS TRANSCEIVER 3
					STATE OUTPUTS
7	3	U5-8 U35	74BCT374		OCTAL D-TYPE FLIP-FLOP
8	1	U26	74HC123		DUAL RETRIGGERABLE
					MONOSTABLE MULTIVIBRATOR
					W/RESET
9	1	U21	74HC4040		12 STAGE RIPPLE CARRY
					BINARY COUNTER
10	1	U23	74HCT245		OCTAL BUS TRANSCEIVER 3
					STATE OUTPUTS
11	1	U18	74HCT374		OCTAL D-TYPE FLIP-FLOP
12	1	U4	AD872		12-BIT 10-MSPS A/D
					CONVERTER, 0.600" 28 PIN
					DIP
13	1	U1	AD9300		4 X 1 WIDEBAND VIDEO
					MULTIPLEXER, 16-PIN CERDIP
14	4	J1-4	BNC		
15	8	U27-30	BNC002		0.5MHz-10Hz 40dB QUADRIPOLE
		U33-34			EMI FILTER, 10AMPS
16	1	U8	BT261		30 MHz PIXEL CLOCK HSYNC
					LINE LOCK CONTROLER, 28PLCC
17	3	C16 C18	CAP+\.1C,1uF		DECOUP CAP RADIAL BODY:.200
		C75			X.200 CENTERS:.100
18	28	C1-8	CAP+\.1C,22uF		DECOUP CAP RADIAL BODY:.200
		C33-34			X.200 CENTERS:.100
		C38-39			
		C58-71			
		C73-74			
19	1	C19	CAP\DM15,100pF		SILVER-MICACAP BODY: .480
					X.180 CENTERS:.225
20	12	C10 C12	CAP\MR04,0.01		CAP RADIAL BODY: .200 X.100
		C14-15			CENTERS: .100
		C17 C21			
		C23 C25			
		C28			
		C30-31			
		C78			
21	34	C9 C11	CAP\MR04,0.1		CAP RADIAL BODY: .200 X.100
		C13 C20			CENTERS: .100
		C22 C24			
		C26-27			
		C29 C32			
		C35-37			
		C40-57			
		C72			
		C76-77			
22	1	J13	CON162P\100\ED		62 FINGERS PCB EDGE
					CONNECTOR, 0.100 SPACING
23	2	J11-12	CON\R1810HL		RIBBON CABLE 10-PIN MALE
					HORIZONTAL LATCHED
24	1	J10	CON\R1840HL		RIBBON CABLE 40-PIN MALE
					HORIZONTAL LATCHED
25	1	U22	CY7C128		2K X 8 BIT HIGH SPEED CMOS

Sheet1

Item	Quanity	Reference
1	1	U31
2	1	U32
3	1	U15
4	1	U12
5	3	U7,U11,U13
6	1	U14
7	3	U5,U6,U35
8	1	U26
9	1	U21
10	1	U23
11	1	U16
12	1	U4
13	1	U1
14	4	J1,J2,J3,J4
15	6	U27,U28,U29,U30,U33,U34
16	1	U8
17	3	C16,C18,C75
18	28	C1-C8,C33,C34,C38,C39,C58-C71,C73, C74
19	1	C19
20	12	C10,C12,C14-15,C17,C21,C23,C25,C28,C30-31,C78
21	34	C9,C11,C13,C20,C22,C24,C26-27,C29,C32,C35-37,C40-57,C72,C76-77
22	1	U22
23	1	Z1
24	1	U2
25	1	U3
26	1	D1
27	1	D2
28	1	U10
29	1	OSC1
30	1	OSC2
31	4	U9,U20,U25,U36,
32	1	U19
33	1	U17
34	3	R8,R10-11
35	1	R35
36	1	R6
37	2	R5,R7
38	1	R20
39	2	R27-28
40	1	R31
41	5	R1-4 R17
42	1	R9
43	8	R12-16,R18-19,R24
44	4	R21-22,R25-26
45	1	R23
46	1	R29
47	1	R30

Sheet1

A	2
B	1
C	2
D	4
E	2
F	1
G	2
H	1
I	10
J	2
K	2
L	2
M	1
N	4

Sheet1

Generic Part Name	Part Number
7805	LT323AT
7905	LM320T-5.0
74ALS520	SN74ALS520N
74AS1004	SN74AS1004AN
74BCT244	SN74BCT244N
74BCT245	SN74BCT245N
74BCT374	SN74ALS374AN
74HC123	74HC123E
74HC4040	MC74HC4040N
74HCT245	M74HCT245B1
74HCT374	SN74HCT374
AD872	AD872JD
AD9300	AD93KQ
BNC	227161-9
BNX002	BNX002-01
BT261	BT261KPJ
1uf	T356A105M035A
22uf	226X9016
100pf	DM15-101J
0,01	CZ15C103M
0,1	CZ20C104M
CY7C128	CY7C128A-55P
Zener	1N821A
EL2090C	EL2090C
KR7B205L-B	7B205LB
Led - RED	551-0407
Led - GREEN	551-0207
LM1882	LM1882CN
Oscillator 14.312 Mhz	14.31818MHz-OSC-F1100H
ME13ZAD 80MHz ECL	ME13ZAD 80MHz ECL
GAL16V8-25	GAL16V8B-25QP
GAL20V8-25	GAL20V8A-25QP
GAL22V8-25	GAL22V10B-25LP
100 ohm 1/4 watt .5"lg	SMA4-100R-1
1 Meg 1/4 watt .5"lg	SMA4-1M-1
2.2K 1/4 watt .5"lg	MRS25F
270 ohm 1/4 watt .5"lg	MRS25F
3.32K 1/4 watt .5"lg	MRS25F
470 ohm 1/4Watt .5"lg	MRS25F
6.82K 1/4 watt .5"lg	SMA4-6.81K-1
75 ohm 1/4 watt .5"lg	MRS25F-75
825 ohm 1/4 watt .5"lg	MRS25F
RESPAK ISO4,4x33ohm 5%	4608X-102-330
RESPAK10p x 9x 10K, 5%	4610X-101-103
RESPAK10p x 9x 150, 5%	4610X-101-151
RESPAK8p x 7x 220, 5%	4608X-101-221
RESPAK8p x 7x 330, 5%	4608X-101-331

Sheet1

TO-220 Heat Sink	5771B
40pin R-A Header	3432-5002
10pin R-A Header	3446-5002
20 pin 0.3 IC Sockets	820-AG11D
24 pin 0.3 IC Sockets	ITC-243-S-TG
28pin PLCC Socket	PCS-028A-1
Rgt Ang terminal strip	TSW-104-08-G-D-RA
Terminal strip	TSW-104-07-G-D
Shunts	SNT-100-BK-G
40 pin socket	3417-6600
10 pin socket	3473-6600
Ribbon Cable 10 Conductor	3365-10
Ribbon Cable 40 Conductor	3365-40
#6-32 Binding HDMS 3/8lg.	

Sheet1

Description	Manufacture	Supplier	Contact
Linear Technology Volt REG +5V, 3 Amp TO-220	Linear Tech	Arrow	Marilyn Brown
National Volt REG -5V 1.5 Amp TO-220	National	Electrosonic	Mitch Gerts
8 Bit Identity Comp	TI	Arrow	Marilyn Brown
Hex Inverting Driver	TI	Future	Andrew MacLaurin
Octal Buffer/Line Driver tri-state	TI	Arrow	Marilyn Brown
Octal Bus Tranceiver tri-state	TI	Future	Andrew MacLaurin
Octal D-Type Flip Flop	TI	Future	Andrew MacLaurin
Dual Retrig Mono Multiv w/reset	Harris	Future	Andrew MacLaurin
12 Stage Ripple Carry Binary Counter	Motorola	Future	Andrew MacLaurin
Octal Bus Tranceiver tri-state	SGS	Future	Andrew MacLaurin
Octal D-Type Flip Flop	TI	Future	Andrew MacLaurin
12Bit 10MIPS A/D Converter	Analog Devices	Future	Andrew
4X1 Wideband Video Multiplexer	Analog Devices	Future	Andrew
Amp PC board BNC Connector	AMP	Electrosonic	Mitch Gerts
0.5MHz-1Ghz 40db Quaripole EMI Filter	Murata-Erie	Future	Andrew
30MHz Pixel Clock Hsync Lock Controler	Brooktree	P.G.Marshall	Carol la Casse
Decoup Cap Radial .2 Tantalum	KEMET	Electrosonic	Mitch Gerts
22uF tantalum radial, +/-20% 16V 0.1Centres	KEMET	Electrosonic	Mitch Gerts
Silver Mica Radial Body .46lgx.18tk centres .225	Miconics	Electrosonic	Mitch Gerts
Cap Radial Body .2 x .1 centres .1	Centralab	Electrosonic	Mitch Gerts
Cap Radial Body .2 x .1 centres .1	Centralab	Electrosonic	Mitch Gerts
2K x 8 Bit High Speed CMOS Static Ram	Cypress	Arrow	Marilyn Brown
6.2V 400mA Low Noise Zener		Electrosonic	Mitch Gerts
100 MHz DC-Restored Video Amp 14 Pin Dip	Elantec	P.G.Marshall	Carol la Casse
2MHz linear phase low pass filter	KR Electronics		Charles J. Kiall
Right angle Red LED	Dialight	Electrosonic	Mitch Gerts
Right angle Green LED	Dialight	Electrosonic	Mitch Gerts
Programmable Video Sync Generator 20 Pin Dip	National	Electrosonic	Mitch Gerts
TTL Crystal Oscillator,14 Pin DIP	FOX	Future	Andrew MacLaurin
	M-Tron Industries	M-Tron Industri	Debbie Loecker
	Lattice	Future	Andrew MacLaurin
	Lattice	Future	Andrew MacLaurin
	Lattice	Future	Andrew MacLaurin
100 ohm metal film 1%	Dale	FAI Electronics	Garry Smith
1M ohm metal film 1%	Dale	FAI Electronics	Garry Smith
2.21K ohm metal film 1%	Philips	Electrosonic	Mitch Gerts
270 ohm metal film 1%	Philips	Electrosonic	Mitch Gerts
3.32K ohm metal film 1%	Philips	Electrosonic	Mitch Gerts
475 ohm metal film 1%	Philips	Electrosonic	Mitch Gerts
6.8K ohm metal film 1%	Dale	FAI Electronics	Garry Smith
Philips 75 ohm metal film 1%	Philips	FAI Electronics	Garry Smith
825 ohm metal film 1%	Philips	Electrosonic	Mitch Gerts
Resistor network 4 isolated 8 pin SIP .1 spacing	Bourns	Electrosonic	Mitch Gerts
Resistor network 9connected 10 pin SIP .1 spacing	Bourns	Electrosonic	Mitch Gerts
Resistor network 9connected 10 pin SIP .1 spacing	Bourns	Electrosonic	Mitch Gerts
Resistor network 7connected 8 pin SIP .1 spacing	Bourns	Electrosonic	Mitch Gerts
Resistor network 7connected 8 pin SIP .1 spacing	Bourns	Electrosonic	Mitch Gerts

Sheet1

TO-220 heat sink	3M-Scotchflex	FAI Electronics	Garry Smith
40pin R-A Header	3M-Scotchflex	Electrosonic	Mitch Gerts
10pin R-A Header	Augat	Electrosonic	Mitch Gerts
20 Pin open frame precision socket	Augat	FAI Electronics	Garry Smith
24 Pin open frame precision socket	Augat	Future	Andrew MacLaurin
Augat 28pin PLCC socket	Samtec	Electrosonic	Mitch Gerts
.025 sq Right angle terminal strip double row 8 pins	Samtec	Carsten	Jan Campbell
.025 sq terminal strip double row 8pins	Samtec	Carsten	Jan Campbell
.1 centres, gold plated shunts	3M-Scotchflex	Carsten	Jan Campbell
40 pin socket	3M-Scotchflex	Electrosonic	Mitch Gerts
10 pin socket	3M	Electrosonic	Mitch Gerts
10 Conductor Ribbon Cable	3M	Electrosonic	Mitch Gerts
40 Conductor Ribbon Cable		Electrosonic	Mitch Gerts

Sheet1

Quote Reqs'd	Quote Rec'd	Lead time	Minimum Order	Item Cost US$	Item Cost CDN$	Cost per Unit	Order Date Units Req'd>>
May 25/94	May 25/94	stock			$ 3,08	$ 3,08	
May 12/94	May 12/94	stock			$ 2,70	$ 2,70	94/05/17
May 12/94	May 12/94	2-3 days			$ 1,68	$ 1,68	94/05/18
May 12/94	May 13/94	stock			$ 0,60	$ 0,60	94/05/13
May 12/94	May 12/94	2-3 days			$ 1,73	$ 5,19	94/05/13
May 12/94	May 13/94	stock			$ 1,97	$ 1,97	94/05/13
May 12/94	May 13/94	stock			$ 0,70	$ 2,10	94/05/13
May 12/94	May 13/94	stock			$ 0,70	$ 0,70	94/05/13
May 12/94	May 13/94	stock			$ 0,88	$ 0,88	94/05/13
May 12/94	May 13/94	stock			$ 0,78	$ 0,78	94/05/13
May 12/94	May 13/94	stock			$ 0,84	$ 0,84	94/05/13
May 10/94	May 11/94	Stock			$ 319,00	$319,00	94/05/13
May 10/94	May 11/94	5 days			$ 18,17	$ 18,17	94/05/13
May 27/94	May 27/94	Stock			$ 4,40	$ 17,60	May 27/94
May 10/94	May 11/94	Stock			$ 5,63	$ 33,78	94/05/13
May 10/94	May 10/94	Stock			$ 29,77	$ 29,77	94/05/12
May 12/94	May 12/94	Stock			$ 0,17	$ 0,51	94/05/17
May 27/94	May 27/94	4 weeks			$ 0,33	$ 9,24	May 27/94
May 27/94	May 27/94	Stock			$ 0,38	$ 0,38	May 27/94
May 12/94	May 12/94	Stock			$ 0,14	$ 1,68	94/05/17
May 12/94	May 12/94	Stock			$ 0,14	$ 4,76	94/05/17
May 12/94	May 12/94	2-3 days			$ 4,75	$ 4,75	94/05/18
May 27/94	May 27/94	stock			$ 0,30	$ 0,30	94/05/27
June 1/94	June 1/94	2 weeks			$ 9,60	$ 9,60	94/05/13
May 10/94	May 10/94	2-4 weeks		$ 45,00	$ 58,50	$ 58,50	94/05/12
May 12/94	May 12/94	2-3 days			$ 0,81	$ 0,81	94/05/17
May 12/94	May 12/94	2-3 days			$ 0,81	$ 0,81	94/05/17
May 12/94	May 12/94	2-3 days			$ 9,20	$ 9,20	94/05/17
May 10/94	May 11/94	5 days			$ 8,00	$ 8,00	94/05/13
May 10/94	May 10/94	2 days		$ 46,37	$ 60,28	$ 60,28	94/05/12
May 13/94	May 13/94	stock			$ 1,49	$ 5,96	94/05/13
May 13/94	May 13/94	stock			$ 2,06	$ 2,06	94/05/13
May 13/94	May 13/94	stock			$ 3,96	$ 3,96	94/05/13
May 12/94	May 12/94	stock			$ 0,07	$ 0,21	94/05/19
May 12/94	May 12/94	stock			$ 0,07	$ 0,07	94/05/19
May 27/94	May 27/94	stock			$ 0,06	$ 0,06	94/05/27
May 27/94	May 27/94	stock			$ 0,06	$ 0,12	94/05/27
May 27/94	May 27/94	stock			$ 0,06	$ 0,06	94/05/27
May 27/94	May 27/94	stock			$ 0,06	$ 0,12	94/05/27
May 12/94		stock			$ 0,07	$ 0,07	94/05/19
May 12/94	May 12/94	stock			$ 0,07	$ 0,35	94/05/19
May 12/94	May 27/94	stock			$ 0,06	$ 0,06	94/05/27
May 27/94	May 27/94	4 weeks			$ 0,20	$ 1,60	94/05/27
May 12/94	May 12/94	stock			$ 0,54	$ 2,16	94/05/17
May 12/94	May 12/94	stock			$ 0,54	$ 0,54	94/05/17
May 12/94	May 12/94	stock			$ 0,45	$ 0,45	94/05/17
May 12/94	May 12/94	stock			$ 0,45	$ 0,45	94/05/17

Sheet1

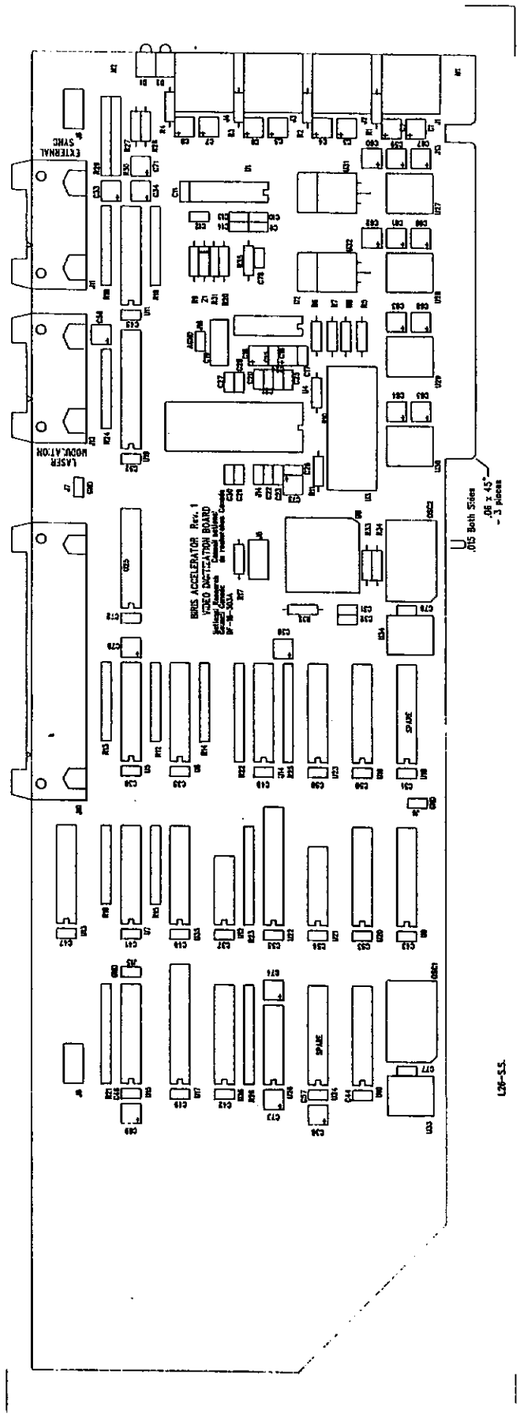
May 12/94	May 12/94	stock			$ 0,20	$ 0,40	94/05/19
May 12/94	May 12/94	stock			$ 4,52	$ 4,52	94/05/17
May 12/94	May 12/94	stock			$ 2,04	$ 4,08	94/05/17
May 12/94	May 12/94	stock			$ 0,71	$ 2,84	94/05/19
July 11/94	July 12/94	stock			$ 0,71	$ 1,42	94/05/19
May 12/94	May 12/94	4 weeks			$ 1,92	$ 1,92	94/05/17
May 12/94	May 12/94	2 weeks			$ 0,35	$ 0,70	94/05/13
May 12/94	May 12/94	2 weeks			$ 0,30	$ 0,30	94/05/13
May 12/94	May 12/94	2 weeks			$ 1,48	$ 14,75	94/05/13
May 12/94	May 12/94				$ 6,35	$ 12,70	94/05/17
May 12/94	May 12/94				$ 2,25	$ 4,50	94/05/17
May 12/94		Stock			$ 0,29	$ 0,57	94/07/08
94/07/08		Stock			$ 1,31	$ 1,31	94/07/08
94/07/08		Stock			$ 0,05	$ 0,20	94/07/08
94/07/08							
						$ 676,18	

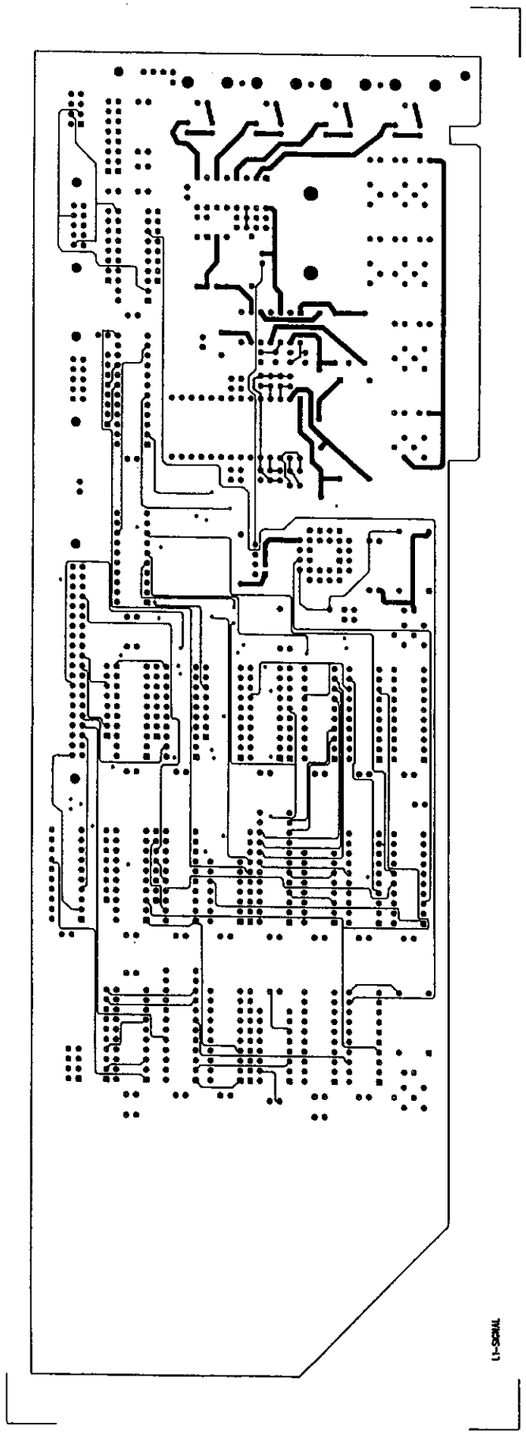
Sheet1

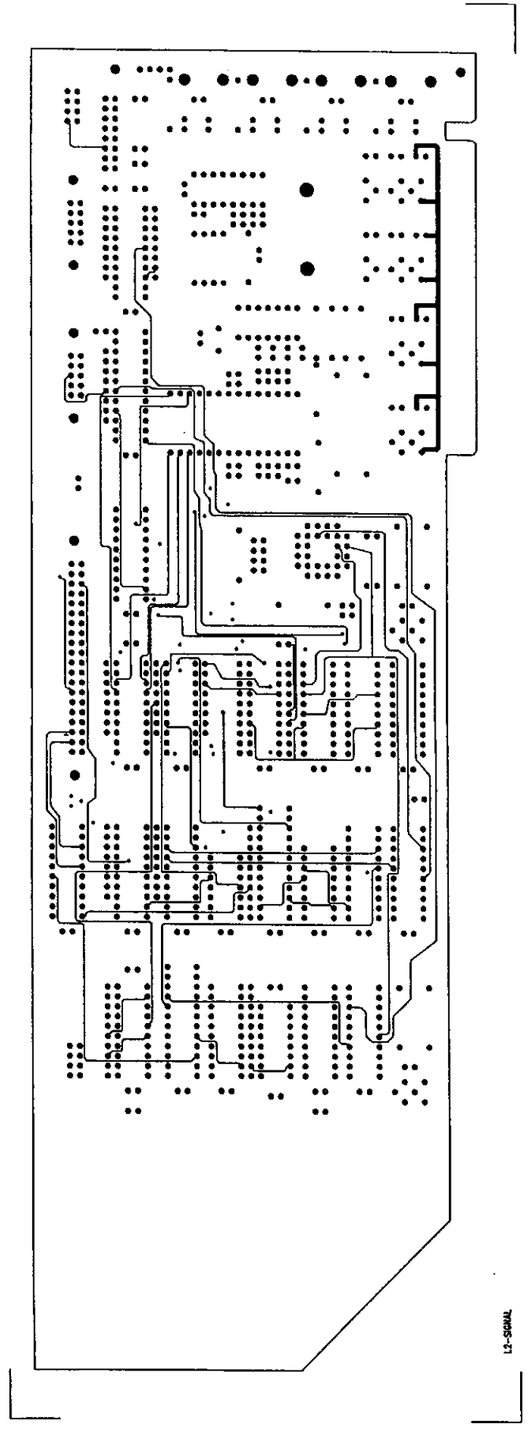
No. of Units	Ordered	Order Cost	Shipment	Back	Order
10	Quanity		Rec'd	Ordered	Complete
10	25	$ 77,00	94/06/08		94/06/08
10	20	$ 54,00	94/05/24		94/05/24
10	20	$ 33,60	94/05/31		94/05/31
10	25	$ 15,00	94/05/24		94/05/24
30	45	$ 77,85	94/05/31		94/05/31
10	20	$ 39,40	94/05/24		94/05/24
30	60	$ 42,00	94/05/24		94/05/24
10	25	$ 17,50	94/05/24		94/05/24
10	25	$ 22,00	94/05/24		94/05/24
10	20	$ 15,60	94/05/24		94/05/24
10	18	$ 15,12	94/05/24		94/05/24
10	15	$ 4 785,00	94/05/25		94/05/25
10	15	$ 272,55	94/05/25		94/05/25
40	50	$ 220,00	94/06/10		94/06/10
60	100	$ 563,00	94/05/24		94/05/24
10	20	$ 595,40	94/06/08		94/06/08
30	100	$ 17,00	94/05/24		94/05/24
280	350	$ 115,50	94/06/10	18	
10	25	$ 9,50	94/06/10		94/06/10
120	200	$ 28,00	94/05/24		94/05/24
340	500	$ 70,00	94/05/24		94/05/24
10	20	$ 95,00	94/05/31		94/05/31
10	15	$ 4,50	94/06/10		94/06/10
10	25	$ 240,00			
10	20	$ 1 170,00			
10	20	$ 16,20	94/05/24		94/05/24
10	20	$ 16,20	94/05/24		94/05/24
10	20	$ 184,00	94/05/24		94/05/24
10	15	$ 120,00	94/05/25		94/05/25
10	20	$ 1 205,62	94/05/31		94/05/31
40	80	$ 119,20	94/05/24		94/05/24
10	20	$ 41,20	94/05/24		94/05/24
10	20	$ 79,20	94/05/24		94/05/24
30	100	$ 7,00			
10	100	$ 7,00	94/05/30		94/05/30
10	100	$ 6,00	94/06/10		94/06/10
20	100	$ 6,00	94/06/10		94/06/10
10	100	$ 6,00	94/06/10		94/06/10
20	100	$ 6,00	94/06/10		94/06/10
10	100	$ 7,00	94/05/30		94/05/30
50	100	$ 7,00	94/05/30		94/05/30
10	100	$ 6,00	94/06/10		94/06/10
80	100	$ 20,00			
40	100	$ 54,00			
10	25	$ 13,50	94/05/24		94/05/24
10	25	$ 11,25	94/05/24		94/05/24
10	25	$ 11,25	94/05/24		94/05/24

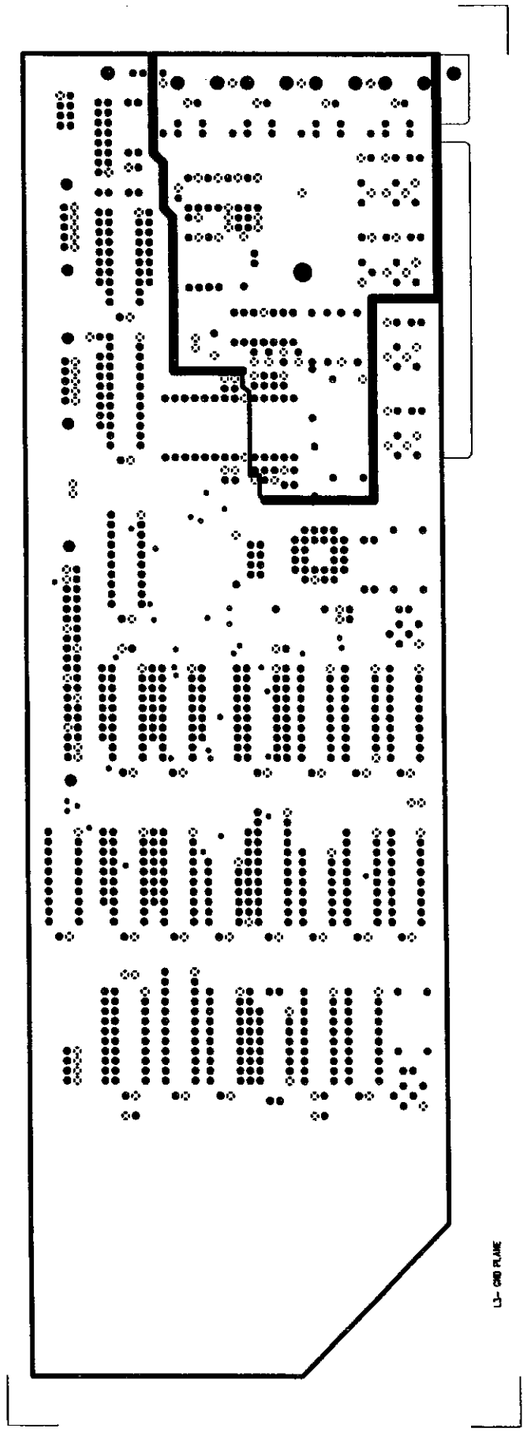
Sheet1

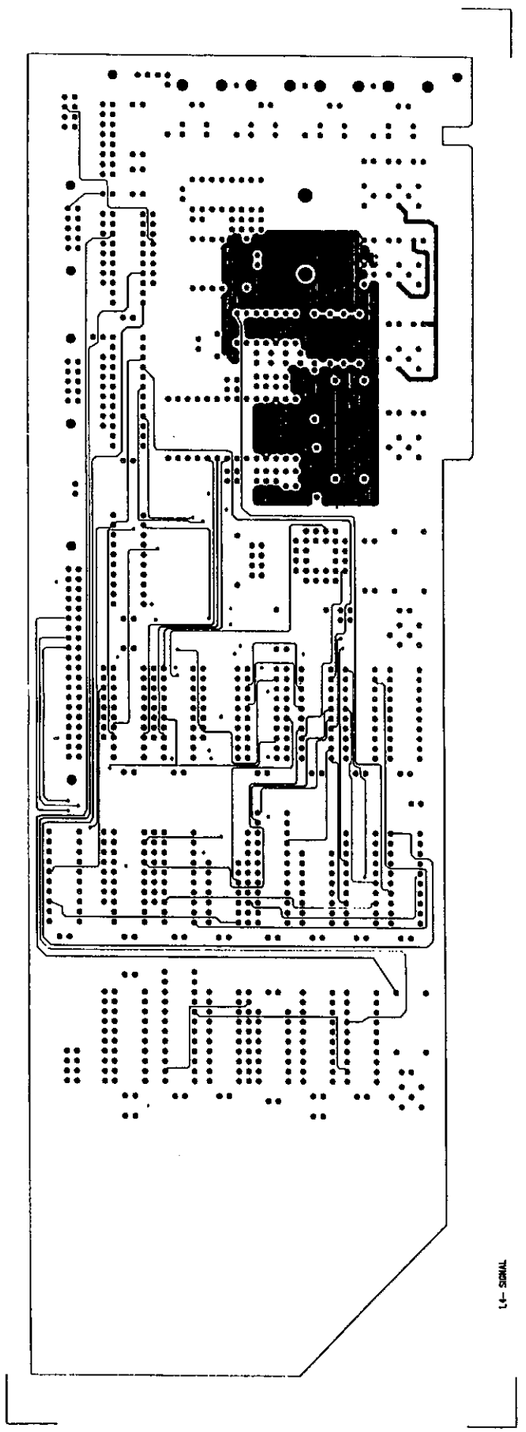
20	30	$	6,00	94/06/10		94/06/10
10	15	$	67,80	94/05/24		94/05/24
20	30	$	61,20	94/05/24		94/05/24
40	50	$	35,50	94/05/30		94/05/30
20	30	$	21,30	94/05/30		94/05/30
10	20	$	38,40	94/05/24		94/05/24
20	50	$	17,50	94/05/30		94/05/30
10	50	$	15,00	94/05/24	35	94/05/30
100	50	$	73,75	94/05/24		94/05/24
20	15	$	95,25			
20	30	$	67,50	94/05/24		94/05/24
20	100	$	28,56			
10	25	$	32,84			
40	100	$	5,00			

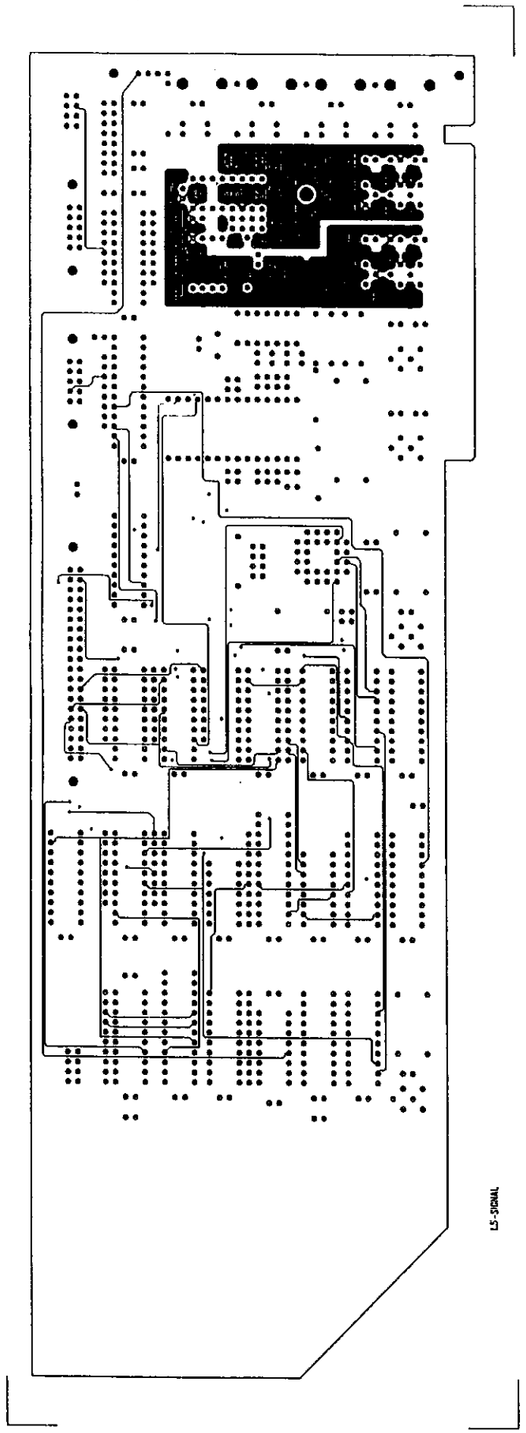


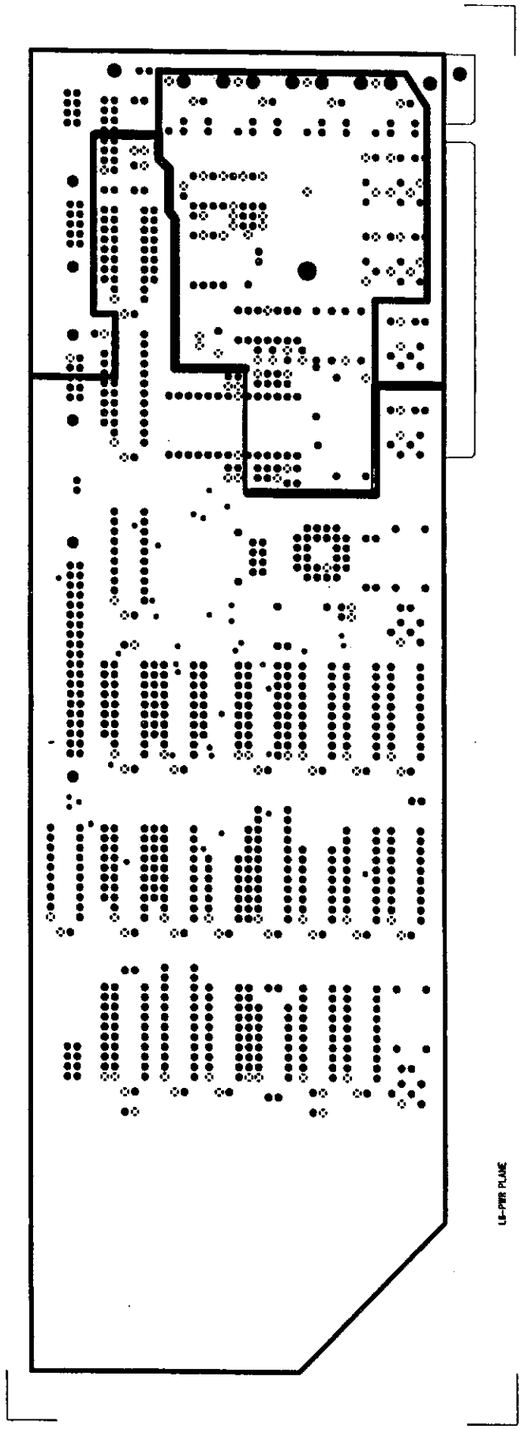

June 8, 94
TWOS-L1

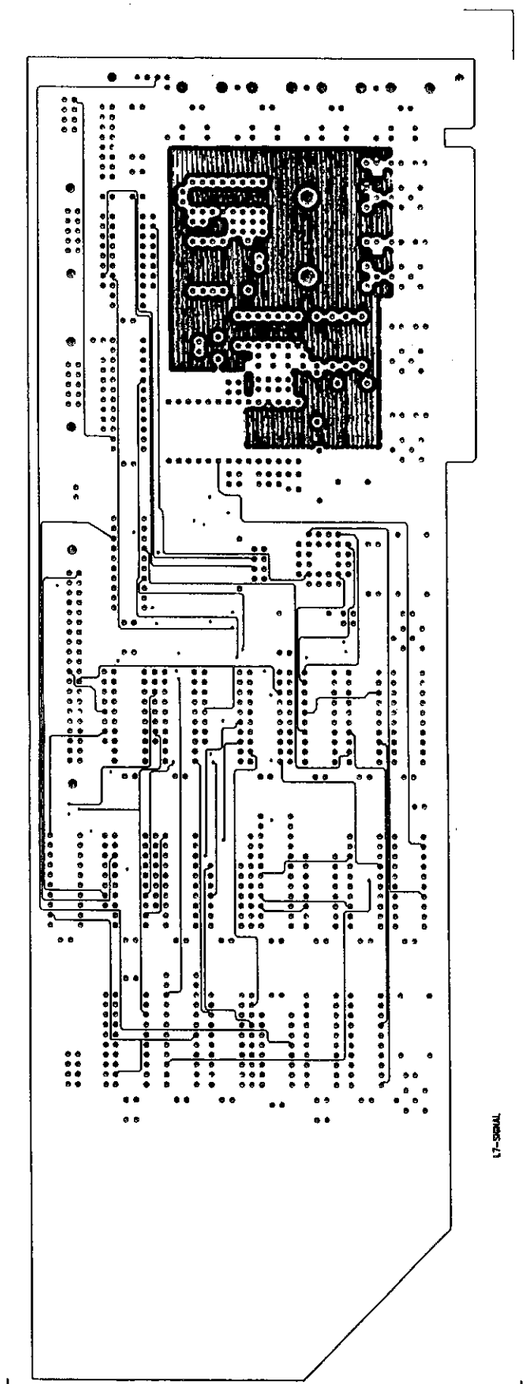

June 8, 94
L2-SIGNAL

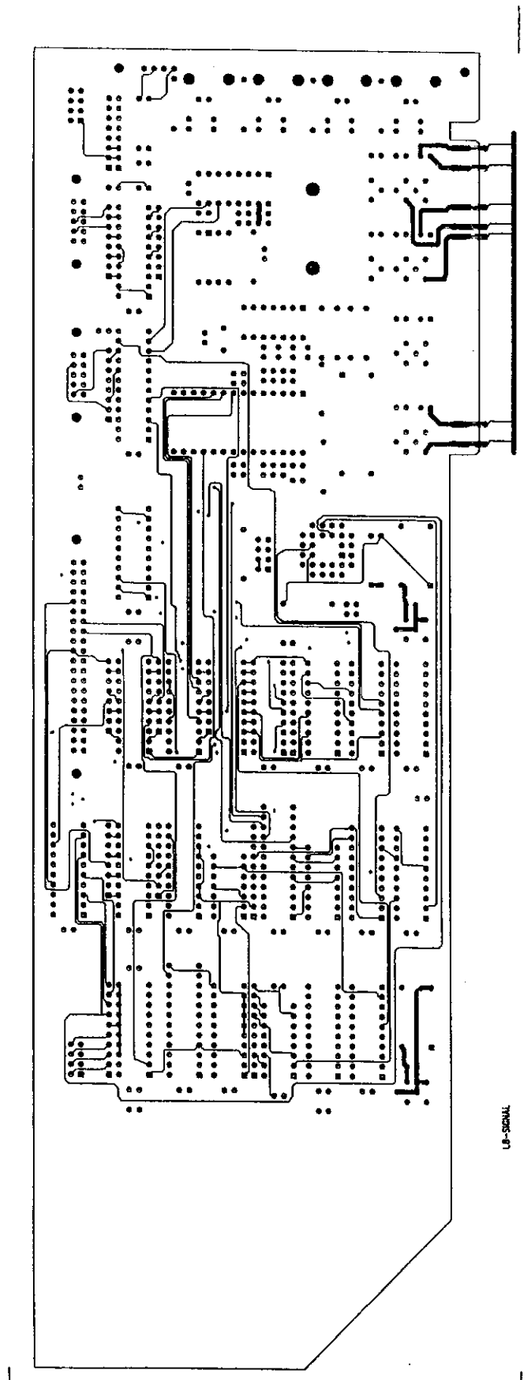

June 8, 94
L3- GND PLANE

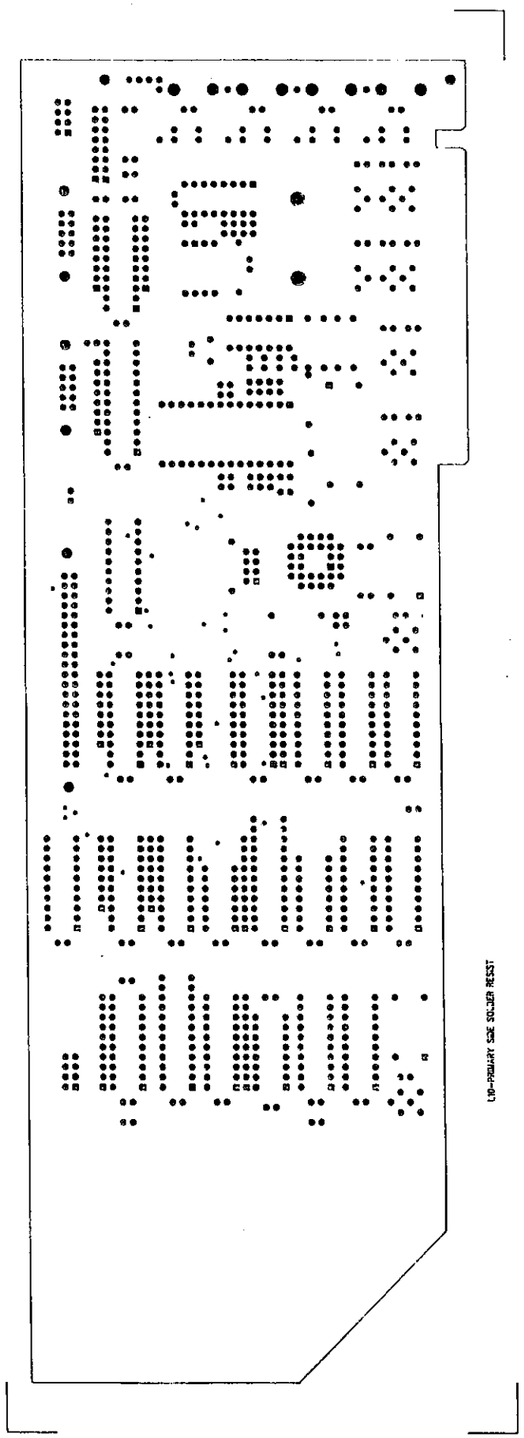

June 8, 94
L4- SIGNAL

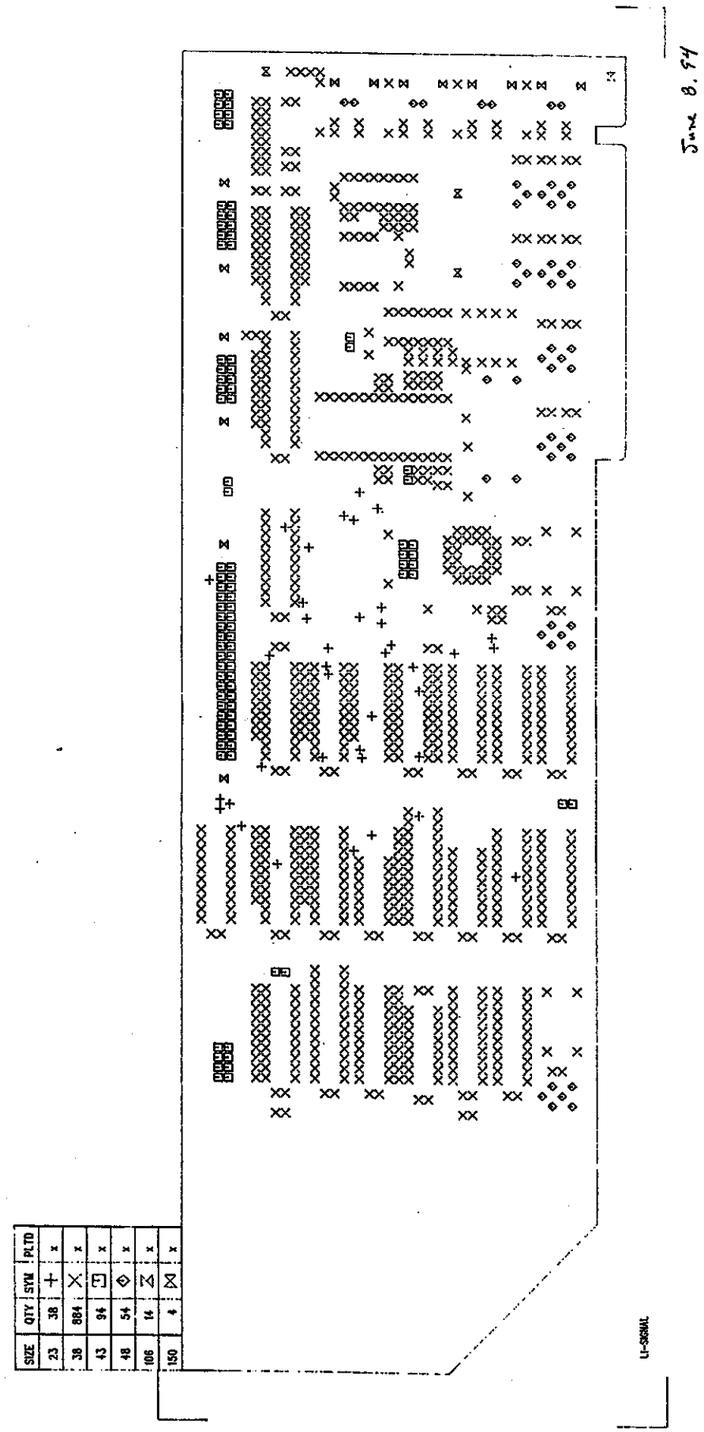

June 8, 94
L5-SIGNAL


June 8, 94
L6-PWR PLANE


June 8, 94
TM36C-L1


June 8, 94
TM36C-B1





SIZE	QTY	SYM	PLTD
23	38	+	x
38	884	X	x
43	94	□	x
48	54	◇	x
106	14	▽	x
150	4	⊠	x

Addendum. VDB Hardware Variations

The BIRIS sensor prototype developed in partnership with Cognitiative System Inc (CSI) in November 1994 includes a new signal called LASER_ENABLE. This active high TTL signal enables the laser power emission. The laser circuitry of the sensor requires a rising edge *after* power-up.

The VDB design in its original version does not support this extra signal. It must be modified to support the new signal. Fortunately a simple solution exists:

- the connector J12 signals are redefined
- the default strapping of J6 pins 7-8 is changed to jumper out
- the PAL U19 P30304 must be replaced (or reprogrammed) with P30306
- the software driver must be modified

Connector J12 modifications:

Original pin out				New pin out			
GND	1	2	LASER_MOD0	GND	1	2	LASER_MOD0
GND	3	4	LASER_MOD1	GND	3	4	LASER_MOD1
GND	5	6	LASER_MOD2	GND	5	6	LASER_MOD2
GND	7	8	LASER_MOD3	GND	7	8	LASER_ENABLE
GND	9	10	+12 V	GND	9	10	+12 V

After power up the LASER_ENABLE is inactive low (the jumper j6 pin 7-8 removed defines the signal as active high).

PAL P30306

The PAL routes the control register 0 bit 2 LASER_DISABLE with inversion to J12 pin 8 LASER_ENABLE.

Also, the LASER_MOD<2:0> states are now independent of the video channel selected. Their states depend on the patterns programmed into the Vertical LUT gated with the LASER_DISABLE signal from the control register 0 bit 2.

The original PAL P30304 allowed the active modulation of only one laser corresponding to the selected video channel. This had to be changed for two reasons. First, with the new modifications, only three modulation signals are available for four video inputs. Second, to switch video channels in real time, the laser power for a particular sensor has to be modulated one field before the channel switching occurred. The Sensor CCD integrates the illuminated scene on one field and outputs the analog video signal on the next field.

Hardware Restrictions

As before, the modulation patterns must be programmed into the Vertical LUT while no acquisition is in progress. The video digitization must be stopped to program the VLUT, since the VLUT is also used to generate the VROI signal.

If realtime switching between several sensors is required, then all laser modulation signal patterns should be programmed into the VLUT and all lasers will be activated at all times while acquiring range data.

The Future

A new PCB will be design to generate the laser modulation signals. This will be a small PCB inserted into the free 8-bit slot available beside the DPB module.

Preliminary Functional Specs:

- The new board will be connected to the DPB register bus and its registers will be mapped into the transputer memory space of the DPB.
- 4 TTL laser modulation signals.
- 4 TTL laser enable signals.
- The laser modulation patterns can be programmed in real time while acquisition is running.
- The registers of the board will be double-buffered and the new programmed values will be effective on the next VRESET/ falling edge. This will remove the burden of writing time critical code.
- The board will be mapped on the PC/AT I/O bus. I/O registers can be programmed to generate interrupts to the PC/AT on a VRESET. The PC/AT interrupt routine can write a 32-bit value in a stamp register. This 32-bit stamp will be attached to the range data vector that will be created for the current video acquisition. When the user's application receives the range data vector at a later time, it will be possible to associate the data with and external event (the position of the Sensor for example).

This board will have two female DB-9 connectors to drive the TTL signals and +12 V power to two BIRIS sensors with the following pinout:

Female DB-9 5 4 3 2 1
Front view 9 8 7 6

DB-9 pin 1: GND
DB-9 pin 2: GND
DB-9 pin 3: LASER MODULATION
DB-9 pin 4: LASER ENABLE
DB-9 pin 5: +12 V
DB-9 pin 6: HORIZONTAL DRIVE
DB-9 pin 7: VERTICAL DRIVE
DB-9 pin 8: GND
DB-9 pin 9: GND

Until this new laser modulation board exists, one can use the modified VDB board to supply all signals to the DB-9 connectors from a combination of signals from the VDB connectors J11 and J12.

Female DB-9		Modified VDB (with U19 PAL P30306)	
1:	GND	J11-3:	GND
2:	GND	J11-5:	GND
3:	LASER MODULATION	J12-X:	LASER_MOD<2:0> (X= pin 2,4, 6)
4:	LASER ENABLE	J12-8:	LASER_ENABLE
5:	+12 V	J12-10:	+12 V
6:	HORIZONTAL DRIVE	J11-4:	HDRIVE
7:	VERTICAL DRIVE	J11-6:	VDRIVE
8:	GND	J12-7:	GND
9:	GND	J12-9:	GND

Note that the total current supply by the +12 V power source to all BIRIS sensors is limited to a total of 1.3 A maximum. The VDB J12 pin 10 +12 V power is coming from the PC/AT bus. The PC/AT bus specification allows a maximum of 1.5 A per 8-bit slot used and the VDB requires 0.2 A for its circuitry.