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ABSTRACT

Enabled by technological improvements, photonic devices and circuits are becoming increasingly more complex. Non-trivial geometries are designed to reduce device footprint, improve performance, and introduce novel functionalities. However, the number of design variables required to properly represent these geometries quickly grows, limiting the effectiveness of classical design approaches. Moreover, parameters are often strongly interdependent, restricting the use of sequential optimizations or independent parameter sweeps. Although several optimization techniques can be effective for multi-parameter design, they commonly allow to optimize for a single or a handful designs and the optimization process needs to be repeated if new performance criteria are introduced. In contrast to classical design approaches, the influences of the design parameters remain hidden as well as the general behavior of the design space. In this paper we present an extension of our recent work on the application of machine learning pattern recognition to the design of multi-parameter photonic devices. In particular, we propose using a combination of local optimization based on the adjoint method and the use of dimensionality reduction. Adjoint optimization is used multiple times to generate a small set of different designs with high performance. Dimensionality reduction is applied to analyze the relationship between these degenerate designs and identify a lower-dimensional design sub-space that includes all alternative good designs. This sub-space can be mapped for any performance criteria thus enabling informed decisions based on the relative priorities of all relevant performance specifications. As a proof of concept, we demonstrate a ten-parameter design of an integrated photonic power splitter using silicon-on-insulator technology. We identify a region of possible high performance design solutions and select two design candidates either maximizing the splitter efficiency or minimizing back-reflection.

Keywords: Inverse design, adjoint method, space mapping, photonics

1. INTRODUCTION

In modern integrated photonics, there is a growing interest in devices with complex geometries that cannot be easily described and designed using classical approaches. A notable example is the surging use of subwavelength meta-materials[1] in guided-wave photonics. Devices using a "solid" core but non-trivial layout are also being investigated.[2] Complex, non-trivial devices are sought to improve performance,[3] scale down dimensions,[4,5] or to obtain functionalities that would otherwise require larger circuits.[6] Such devices often require a large number of parameters to be properly described. In this scenario, sequential optimization is unlikely to succeed and simultaneous optimization of multiple parameters is required. Inverse design based on shape[7] or topology

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optimization[4,8,9] has emerged as a promising approach to handle complex device design.[10] In particular, the use of gradient-based algorithms in combination with adjoint simulations has been demonstrated to be particularly efficient in exploring large design spaces.[8,11–13] Although extremely powerful, adjoint optimization remains a local optimization technique which makes the choice of the initial guess for the parameter set critical to avoid local minima and properly converge to the global optimum. This problem can be partially mitigated by exploiting, for example, a hierarchical approach to generate promising initial guesses for the optimization.[14] Alternatively, optimizers such as genetic and particle swarm algorithms can be used to increase the chances to reach the global optimum.[15] Neural-network-based approaches are also being extensively explored to speed-up the search process.[16] However, other limitations remain. In particular, the co-optimization of multiple performance criteria is non-trivial and requires the user to carefully craft and weigh several terms in the objective function to obtain the desired result. Moreover, only a single or a handful of optimized designs are discovered, revealing very little on the characteristics of the design space and the influence of the design parameters on the device performance.

Pattern recognition by dimensionality reduction is a class of techniques that allows to identify relations between design parameters, scaling down the problem complexity and consequently computational resources.[17,18] Recently, we proposed a method exploiting dimensionality reduction to effectively map and characterize multiparameter design spaces.[17] From an initial sparse set of optimized designs, principal component analysis is used to identify the lowest number of independent parameters that still properly describe designs with high-performance. The use of this optimization methodology does not require a careful choice of the initial guess to confidently search for the global optimum of a particular performance criterion. Moreover, any additional criteria can be efficiently evaluated in the reduced design sub-space only, without implementing complex objective functions and enabling the discovery of superior designs based on the design constraints and performance requirements of interest. In this paper, we introduce an extension of this approach to use inverse design based on a local optimizer in combination with adjoint simulations.[7] This allows to handle a larger number of initial parameters and still efficiently generate the sparse set of good designs required to perform dimensionality reduction. We demonstrate this methodology analysing the design space of a 1x2 power splitter in the silicon-on-insulator (SOI) platform whose profile is described by ten parameters. By comprehensively mapping the design space we are able to identify very different designs with similar efficiency but rather different behaviours when other criteria, e.g. back-reflections or operational bandwidth, are considered.

2. GLOBAL DESIGN SPACE MAPPING AND ADJOINT METHOD

In order to efficiently map device performance on a multiparameter design space, we exploit a design methodology based on three main steps summarized in Fig. 1. For a given device design with M parameters, a primary performance criterion is chosen, e.g., efficiency in the case of the power splitter described in Section 3. The goal of the first step is to sample the original M-dimensional design space of the device to generate a sparse collection of different designs that optimize the primary performance criterion. This is done by generating a number of guess designs, described by parameter sets $[p_1, p_2, \ldots, p_M]$. The subsequent optimization process can be made more efficient by selecting among this random collection only the designs with performance above a minimal threshold. This requires at most a single additional simulation and allows the optimization to start only from the most promising guesses. If a surrogate model is available, a supervised machine-learning predictor can also be used to rapidly screen out random designs without performing any simulation.[17] These designs are then used as initial guesses for a local adjoint optimization. We use the open source package lumopt from Lumerical[19] based on box-constrained limited-memory Broyden–Fletcher–Goldfarb–Shanno algorithm (L-BFGS-B) and finite difference time domain (FDTD) simulations. Parameter values are box constrained to avoid nonphysical designs. As expected, the quality of each end design generated by the optimizer in terms of the selected performance criterion strongly depends on the initial guess and often local optima are found.

In the second stage, only the optimized designs whose performance is above a given threshold are considered. Depending on the specific design problem, this threshold is used to filter out local optima that are far from the region of the design space where the best performing (and interesting) designs reside. Linear principal component analysis is then applied as the dimensionality reduction algorithm to analyze the relationship in the M-dimensional parameter space between these designs. The goal is to find a lower-dimensional sub-space described by significantly fewer parameters (N) than the original design space (described by M parameters). In

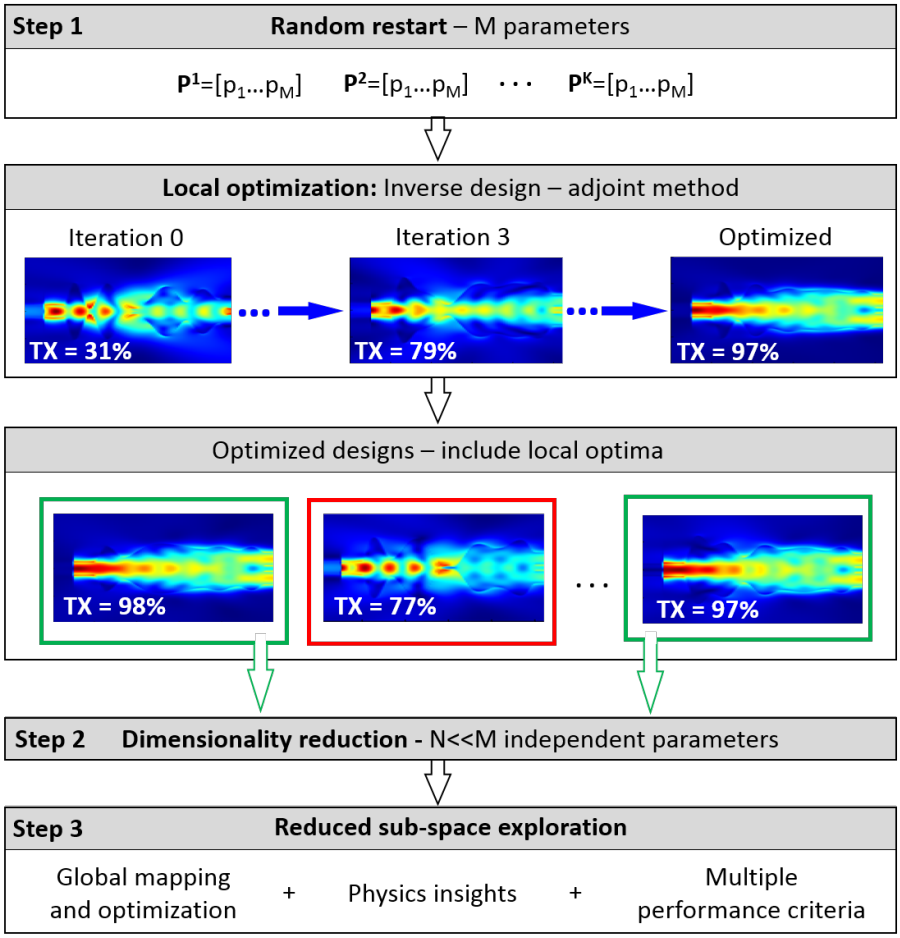

Figure 1. Overview of the proposed design methodology based on dimensionality reduction. A number of random restarts are used as initial guess for the local optimization based on adjoint simulations. Only the best locally optimal designs are used as a training set for the dimensionality reduction, which identifies the smallest number of independent design parameters that form the lower-dimensional design sub-space.

the last stage, the new N-dimensional sub-space can be explored by mapping any performance criteria in addition to the original primary one used for the optimization stage. This sub-space is easier to navigate and can be mapped much faster than the original design space. Continuous regions of good designs can be identified and different design solutions can be easily compared. When required, design space maps make the global optimum for a specific performance criterion easy to identify.

3. APPLICATION TO DEVICE DESIGN

As an application example, we consider here the design of an integrated power splitter in the SOI technology whose geometry is schematically shown in Fig. 2(a). The device has one input port and two parallel output ports at a distance of 1 µm. Waveguides are 450 nm wide. The profile of the device is symmetrical in the y direction and is described using 10 sampling points (red dots) placed on a uniform grid along the x axis with a distance of 0.7 µm. The y coordinates of these ten points represent the M = 10 parameters describing the device and are bounded between 0.225 µm and 2 µm, where the maximum allowed width for the device is 4 µm. To generate the layout, a segmented linear interpolation is performed between the ten points. Sharp features are removed by convolution of the obtained profile with a Gaussian function using σ = 100 nm. Simulations are performed with 2D-FDTD in combination with the effective index method. An effective refractive index of 2.8

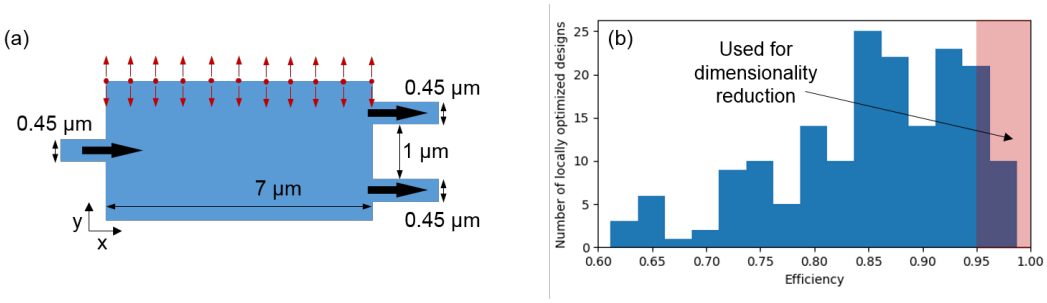

Figure 2. (a) Parametrization of the device geometry. The profile of the power splitter is symmetrical in the vertical direction and is defined by ten sampling points placed on a 0.7-µm-spaced uniform grid. (b) Histogram of the efficiency of the splitter designs generated by the local adjoint optimization. Only designs with efficiency above 0.95 were used for dimensionality reduction.

and 1.44 are considered at a wavelength of 1550 nm for the core and surrounding silica, respectively.

The primary performance criterion used during the initial optimization is the overlap between the field at the output of the optimization region and the fundamental TE symmetric super-mode of the two output waveguides calculated at $\lambda = 1550$ nm (power splitter efficiency). Initial random designs were generated with a uniform parameter distribution within the allowed boundaries and filtered with a preliminary simulation. Of 836 random restarts only 175 had an efficiency larger than 0.35 and were used to seed the local adjoint optimization. Figure 2(b) shows the histogram of the power splitter efficiency for all the resulting designs generated by the adjoint optimization. As can be seen, even with the preliminary filtering, the output of the optimization has a very large variability due to the difficulty in navigating the 10D parameter space and the consequent extreme dependence of the result on the initial guess. In this case, we considered any efficiency below 0.95 as an unacceptable local optimum and discarded the associated design. We retained in total 18 optimized designs. For the principal component analysis, N = 4 dimensions allowed to properly describe the sub-space of these good designs, explaining about 96% of the total variance of the training dataset (the 18 optimized designs). Principal component analysis hence reduced the number of design parameters from the original ten to the four principal component coefficients.

The reduced sub-space described by these four new coefficients was finally mapped generating a uniform grid spanning in each direction three times the standard deviation of the training dataset. The Manhattan distance $d = \sum_{i=1}^{M} |p_i^A - p_i^B|$ between each sampling point in all four directions was set to 500 nm. Each of these points represents a new possible device design. Designs that did not respect the same boundaries used for the initial optimization phase (profile y coordinate comprised between 0.225 µm and 2 µm) were not simulated. For the remaining 5750 designs, we simulated two performance criteria as a function of wavelength: the efficiency and the back-reflection, i.e., the amount of power coupled to the counter-propagating TE mode of the input waveguide.

The results of the mapping are reported in Fig. 3. In order to represent the 4D sub-space, two 3D projections are used. In Fig. 3(a) and (c) efficiency and back-reflection are respectively reported as a function of the first three parameters (principal component coefficients). Figures 3 (b) and (d) show the same data as a function of parameters 1, 2 and 4. To improve readability, in all the graphs the size of the points is proportional to the corresponding device efficiency. The possibility to map the reduced parameter sub-space allows the designer to obtain additional insight into the device behaviour. A large design area with highly efficient devices can be identified (dark red dots in Fig. 3 (a,b)). Despite the fact that, as shown below, the geometrical layout of these devices can be significantly different, they all exhibit similar high efficiency. On the other hand, they may show considerable differences when other performance criteria, e.g., back-reflection, are considered.

Two designs are selected for further examination and are marked as Designs 1 and 2 in Fig. 3. The first one is the design in the reduced sub-space with the largest efficiency at $\lambda = 1550$ nm (about 0.98). The second design has the lowest back-reflection at $\lambda = 1550$ nm among all the designs with efficiency larger than 0.95. Figures 4 (a,b) report the layout of the two power splitters (including also input and output waveguides) and the absolute value of the electric field. As can be seen, the devices are rather different in particular near the

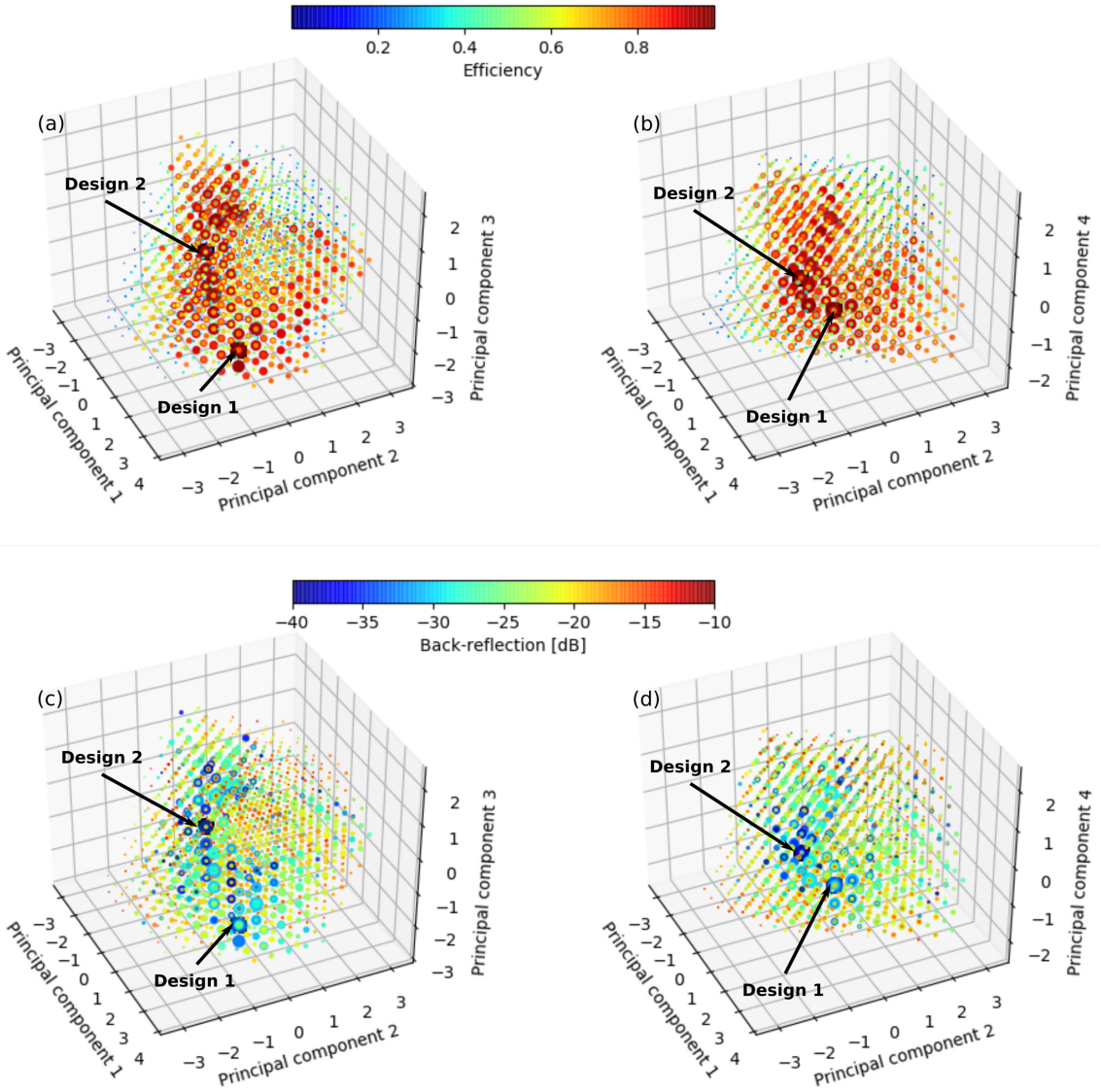

Figure 3. Maps of the 4D sub-space of good designs. In order to visualize the results, two 3D projections are used. (a,b) Power splitter efficiency and (c,d) back-reflection.

input, with a tapered section that is much longer for design 2 than for design 1. Figures 4 (c) and (d) report on the efficiency and back-reflection of the two splitter designs across the fiber communication C band (1530 - 1565 nm), respectively. As already mentioned, design 1 has the largest efficiency at the center of the band (about 0.98) but an absolute drop of about 2.5% can be observed at $\lambda = 1530$ nm. Design 2 has a peak efficiency of 0.97, about 1% lower than design 1. On the other hand, a much more broadband behaviour can be observed with an absolute efficiency fluctuation smaller than 0.5% across the entire C band. The dependence of back-reflection on wavelength is quite similar for the two designs but since design 2 was selected for low back-reflection this is about 10 dB smaller than design 1 across almost the entire C band (about -43 dB at $\lambda = 1550$ nm). Design 1 could therefore be preferable if efficiency must be maximized at the central wavelength while design 2 can provide lower back-reflection and a broader operational bandwidth.

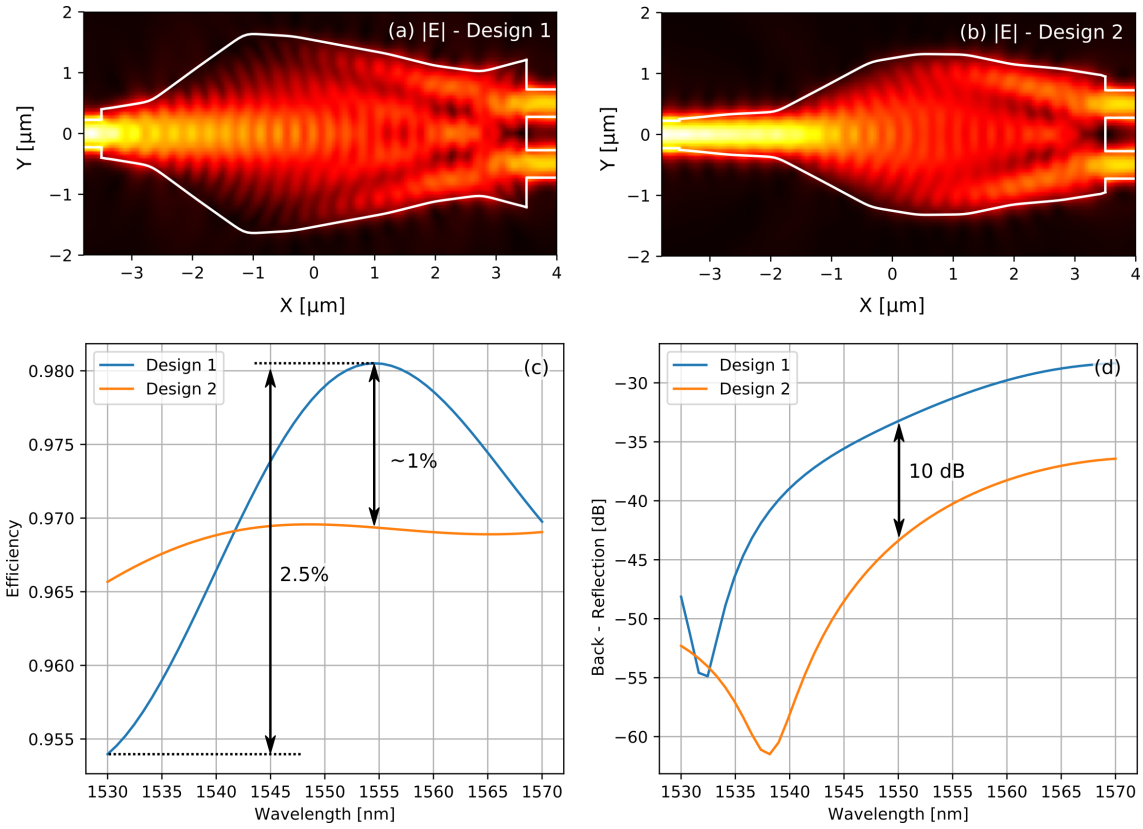

Figure 4. Absolute value of the electric field for (a) design 1 and (b) design 2. The layout of the two devices is superimposed as well. (c) Power splitter efficiency and (d) back-reflection as a function of wavelength.

4. CONCLUSIONS

In this work we have presented a design approach based on the combination of local adjoint optimization and dimensionality reduction. Using the design of a power splitter as a proof of concept, we have shown that this technique can help mitigate the strong initial guess dependence of the result of an adjoint optimization. By reducing the number of design parameters from the initial 10 to a final 4 principal components, we were able to map the design space, discover a large area of highly efficient devices, and co-optimize multiple performance criteria without complex objective functions or additional adjoint optimization runs.

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