Good 150oC Retention and Fast Erase Characteristics in Charge-Trap-Engineered Memory having a Scaled Si3N4 Layer

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Good 150°C Retention and Fast Erase Characteristics in Charge-Trap-Engineered Memory having a Scaled Si_3N_4 Layer

S. H. Lin[a], Albert Chin[b,c], F. S. Yeh[a], and S. P. McAlister[d]

[a] Dept. of Electrical Engineering, National Tsing Hua Univ., Hsinchu, Taiwan, ROC
[b] Dept. of Electronics Engineering,, National Chiao-Tung Univ., Hsinchu, Taiwan, ROC
[c] Nano-Electronics Consortium of Taiwan ROC
[d] National Research Council of Canada, Ottawa, Canada
Tel: +886-3-5731841; Email: albert_achin@hotmail.com

Abstract

We report a new charge-trap-engineered flash non-volatile memory that has combined 5nm Si_3N_4 and 0.9nm EOT HfON trapping layers, within double-barrier and double-tunnel layers. At 150°C under a 100μs and ±16V P/E, this device showed good device integrity of a 5.6V initial ΔV_{th} window and 3.8V 10-year extrapolated retention window. These data are better than the 3.3V initial ΔV_{th} and 1.7V 10-year data for a similar structure not having the extra HfON layer.

Introduction

According to the *International Technology Roadmap for Semiconductors* (ITRS) [1], continuous down-scaling of SONOS non-volatile memory (NVM) [1]-[12] is required by scaling down the charge-trapping layer to <6nm, to suppress short-channel effects. This is challenging since the charge trapping deteriorates when the Si_3N_4 is made thinner - for instance, very little charge trapping was shown for a 2nm Si_3N_4 layer used as the tunnel layer of BE-SONOS [10]. The high temperature retention also gets worse when the Si_3N_4 is thin, due to the higher trap energy in the oxide/Si_3N_4/oxide, arising from quantum confinement. The retention may be improved by using a BE-SONOS structure [10], but this yields low erase speeds (10~100ms). Such a retention and erase-speed trade-off is a fundamental limitation of charge-trap-flash (CTF) NVM. We have addressed this using a deep-trapping Al(Ga)N or HfON layer in a MONOS device [5]-[8]. The retention improves with increasing electron affinity (E_{vac}-E_C), going from Al(Ga)N to HfON. By using an Al(Ga)N trapping layer, rather than Si_3N_4, the retention improves in a SONOS device, as confirmed by Samsung [9]. Here we report a novel charge-trap-engineered flash (CTEF) NVM device. This combines a 5nm Si_3N_4 with a 0.9nm EOT layer of HfON, within double-barrier and double-tunnel layers, and still shows good retention and a large memory window. At 150°C and ±16V program/erase (P/E), the device showed a P/E speed of 100μs, an initial ΔV_{th} window of 5.6V and an extrapolated 10-year retention of 3.8V. These results are much better than those of a control CTF device with a single Si_3N_4 trapping layer, which had a smaller initial ΔV_{th} and poorer 10-year retention. The improvement in the memory window in the new device indicates the better trapping capability of the Si_3N_4-HfON structure, at a penalty of only extra 0.9nm for the EOT. We attribute the improved 150°C retention in the CTEF devices to charges, trapped in shallow-energy traps in the thin Si_3N_4 layer, relaxing into deeper energy ones in the HfON layer, rather than leaking out. The 10^5-cycled window was found to be 4.9V. These results compare well with other data [2]-[12], with respect to the 150°C retention, speed and memory window.

Experimental Details

The layers of the TaN-[SiO_2-$LaAlO_3$]-[Si_3N_4-HfON]-[$LaAlO_3$-SiO_2]-Si CTEF devices comprised 2.5nm of thermal SiO_2, 2.5nm of PVD $LaAlO_3$, 5nm of reactive PVD $HfON_{0.2}$ [13]-[14] and 5nm of Si_3N_4 by LPCVD. Then 8nm $LaAlO_3$ by PVD, 5nm SiO_2 by PECVD, and 200nm TaN by PVD. This was followed by standard gate definition, self-aligned P^+ implantation and an RTA. The $LaAlO_3$ was obtained from mixed Al_2O_3 and La_2O_3 dielectrics, used for V_t tuning and V_{fb} shifting [15]-[20] for 32 nm node high-κ *p*- and *n*-MOSFETs. For comparison, control devices having a single layer of Si_3N_4 CTF, and a similar structure, were made. The devices were measured by P/E, cycling and retention to 150°C.

Results and Discussion

A. P/E Characteristics:

In Fig. 1 we compare, schematically, the conventional MONOS, double-barrier double-tunnel single-Si_3N_4-trapping CTF, and double-barrier double-tunnel double- shallow- and deep-trapping-energy-layer CTEF devices. The use of double $LaAlO_3$-SiO_2 tunnel layers permits a faster P/E. This arises from the ΔE_C and ΔE_V in the $LaAlO_3$/SiO_2 which gives better electron and hole tunneling during the program and erase procedures. The increased physical thickness, arising from the use of a high-κ layer, improves the retention. The addition of HfON in the Si_3N_4-HfON stack provides a deep trapping energy, for only an extra 0.9nm for the EOT. This also improves the retention through charge confinement with respect to the high-κ $LaAlO_3$ layer. Fig. 2 displays the *J*-*V* erase characteristics indicating small leakage up to 150°C. A large *C*-*V* hysteresis of 6.6~9.9V was found under ± 13~17V sweep (Fig. 3). In Figs. 4-5 we show the V_{th} shift for the program and erase cases. A P/E time of 100μs was measured at ±16V, along with a large ΔV_{th}, yielding a memory window of 5.6V in the CTEF device. For comparison, the program

and erase characteristics of a control single-Si_3N_4-trapping CTF device (Figs. 6-7) show that the ΔV_{th} is smaller and has a smaller memory window of 3.3V at ±16V 100μs P/E.

B. Retention & Cycling:

The retention data at 25, 85 and 150°C are displayed in Figs. 8-10. The extrapolated 10-year memory window decreases with increasing temperature. At 150°C, an initial ΔV_{th} of 5.6V and 10-year window of 3.8V were measured at 100μs and ±16V P/E. The 10^2~10^3 times faster erase times, compared with a BE-SONOS design [10], are due to the lower hole tunneling energy barrier, ΔE_V, between the $LaAlO_3$ and the SiO_2 in the CTEF devices. This design is possible due to the existing ΔE_V and ΔE_C between HfON trapping layer and high-κ $LaAlO_3$ tunneling layers for both fast hole tunneling erase and trapped electron retention, respectively. Meanwhile good retention is also maintained by physically thicker double $LaAlO_3$-SiO_2 confinement and that stored charges relax from the shallow-trap-energy in the Si_3N_4 into deeper traps in the HfON [13]-[14] (see Fig. 1(c)). The large 10-year window would allow 4 logic levels, as in multi-level cells (MLC), since there is an average of ~1.3V between the levels at 150°C. For comparison, the retention data of a control device appear in Fig. 11. A 3.3V initial ΔV_{th} and 1.7V 10-year extrapolated memory window were found - much worse than data for the CTEF device. The endurance was good: viz. a large 10^5-cycle window of 4.9V and 10^3-cycled 10-year retention window of 4.1V, at ±16V 100μs P/E (Figs. 12-13). This performance occurs because the rapid P/E produces less stress and trap-generation in the 3nm EOT $LaAlO_3$-SiO_2 tunnel oxide. Table 1 compares and summarizes the memory data. Our CTEF device data compares well with that for other devices [2]-[12], and shows a larger memory window, better 150°C retention and higher speed.

Conclusions

We report a new CTEF NVM device with excellent 10-year extrapolated retention window of 3.8V from an initial 5.6V memory window at 150°C, at 100μs and a ±16V P/E. This was realized by using combined shallow- and deep-trapping layers of Si_3N_4-HfON.

Acknowledgments

The authors at NCTU like to thank Director T. B. Wu at Materials Sci. Eng. Dept., National Tsing Hua University for the help.

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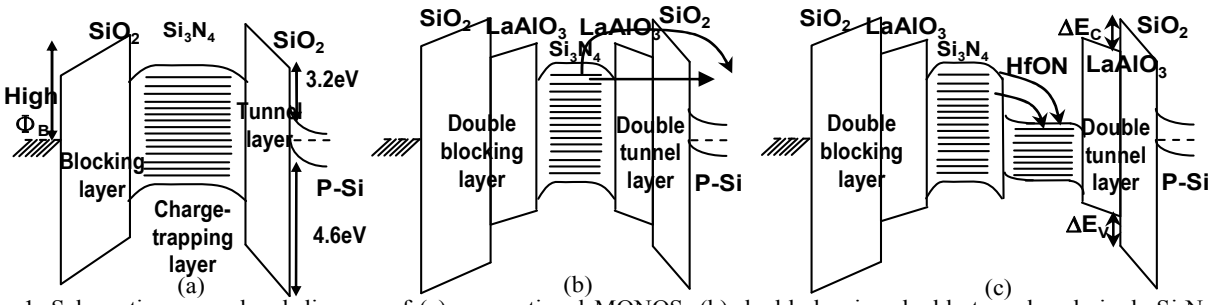

Fig. 1. Schematic energy band diagram of (a) conventional MONOS, (b) double-barrier, double-tunnel and single-Si_3N_4 charge-trapping flash (CTF) memory (control), and (c) charge-trapping-engineered flash (CTEF) non-volatile memory with shallow- and deep- trapping layers and additional ΔE_C in trapping layer to double-tunnel layers (this work).

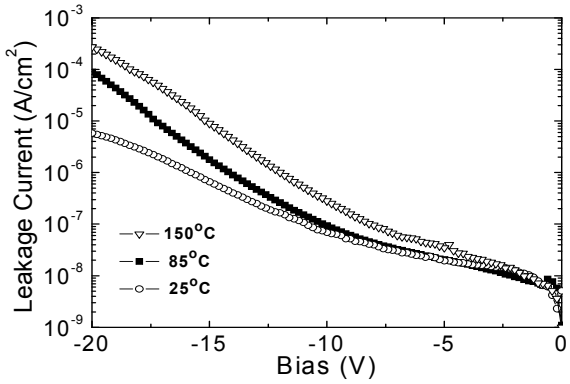

Fig. 2. J_g-V_g curves for CTEF devices.

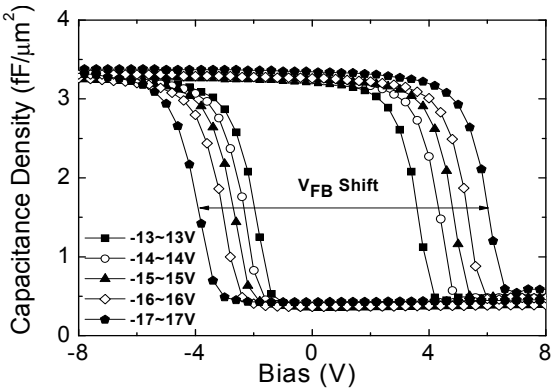

Fig.3. *C-V* hysteresis of CTEF devices.

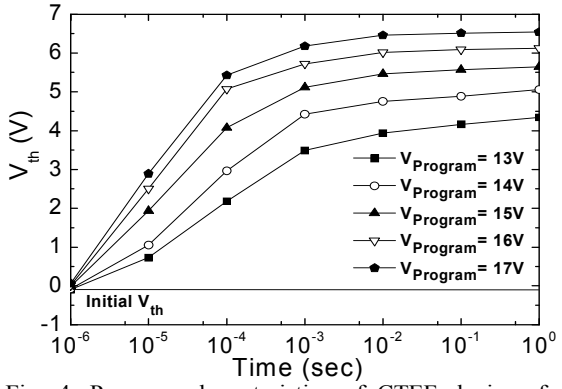

Fig. 4. Program characteristics of CTEF devices for different voltages & times.

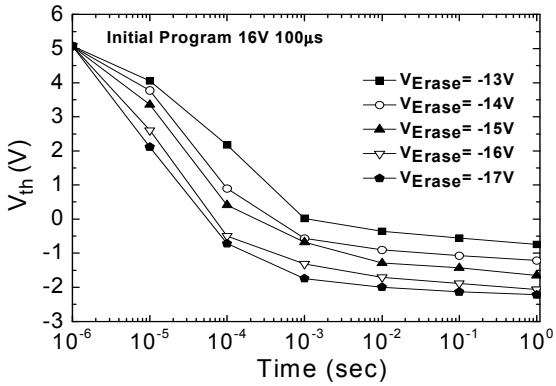

Fig. 5. Erase characteristics of CTEF devices at different voltages & times.

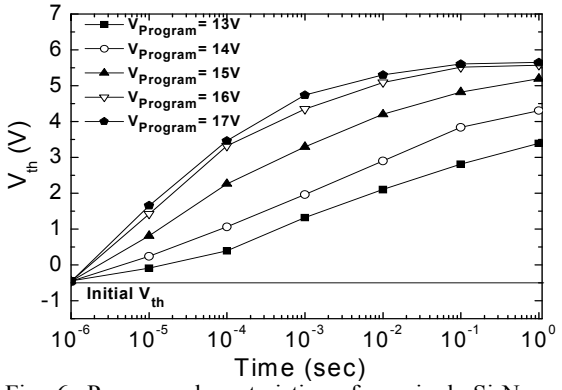

Fig. 6. Program characteristics of a single-Si_3N_4-trapping, double-barrier and double-tunnel CTF device for different voltages & times.

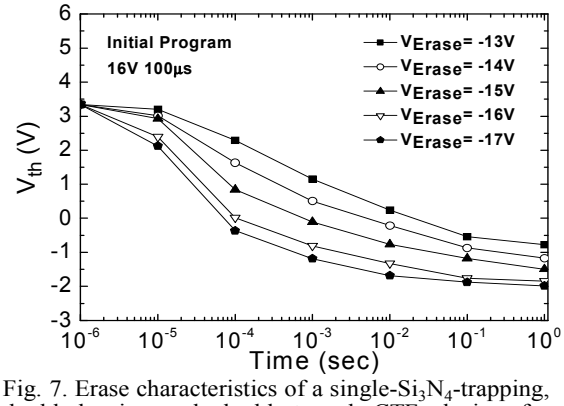

Fig. 7. Erase characteristics of a single-Si_3N_4-trapping, double-barrier and double-tunnel CTF device for different voltages & times.

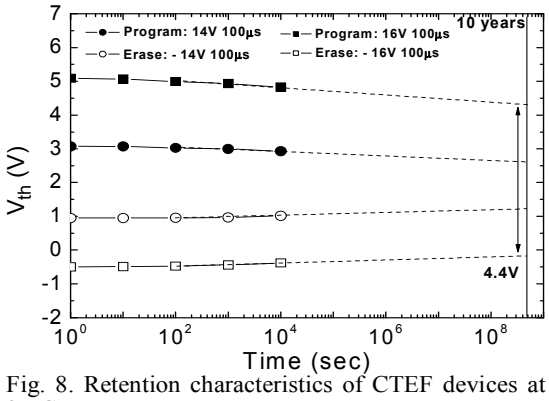

Fig. 8. Retention characteristics of CTEF devices at 25°C.

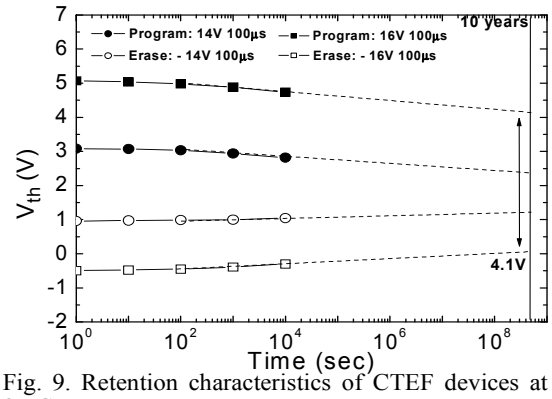

Fig. 9. Retention characteristics of CTEF devices at 85°C.

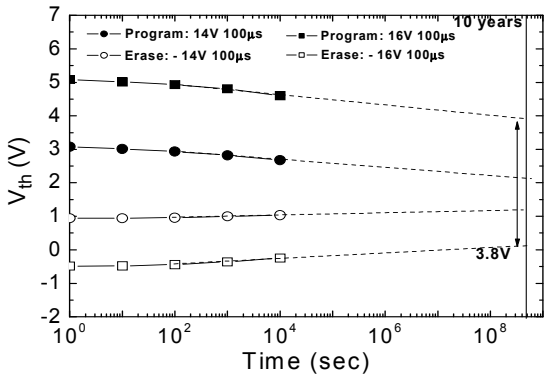

Fig. 10. Retention characteristics of CTEF devices at 150°C.

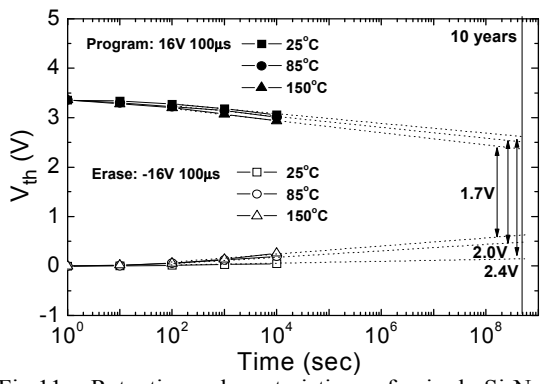

Fig.11. Retention characteristics of single-Si_3N_4-trapping, double-barrier and double-tunnel CTF devices at 25°C, 85°C and 150°C.

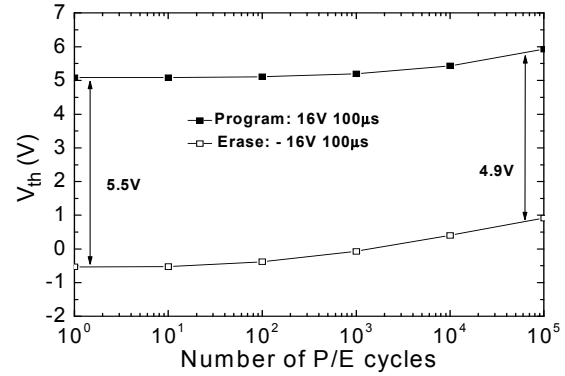

Fig. 12. Endurance characteristics of CTEF devices.

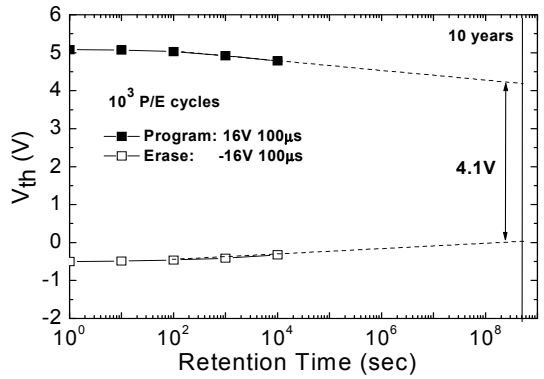

Fig. 13. 1K cycled retention data of CTEF devices.

	P/E conditions for retention & cycling	Initial ΔV_{th} (V)	ΔV_{th} (V) for 10-year retention @ 85°C	ΔV_{th} (V) for 10-year retention @ 150°C	ΔV_{th} (V) @Cycles
This Work (CTEF)	**16V 100µs/-16V 100µs**	**5.6**	**4.1**	**3.8**	**4.9@10^5**
This Work (single-trapping Si_3N_4 CTF)	**16V 100µs/-16V 100µs**	**3.3**	**2.0**	**1.7**	**-**
TANOS $SiO_2/Si_3N_4/Al_2O_3/TaN$ [2]	13.5V 100µs/-13V 10ms	4.4	2.07	-	4@10^5
Tri-gate $SiO_2/Si_3N_4/SiO_2$ [3]	11.5V 3ms/-11.5V 100ms	1.2	1.1 (@25°C)	-	1.5@10^4
FinFET $SiO_2/Si_3N_4/SiO_2$ [4]	13V 10µs/-12V 1ms	4.5	2.4	-	3.5@10^4
SiO_2/AlN/AlHfO/IrO_2 [5]	13V 100µs/-13V 100µs	3.7	1.9	-	2.9 @ 10^5
SiO_2/AlGaN/$AlLaO_3$ [6]	11V100µs/-11V 100µs	3.0	1.6	-	2.3@10^5
SiO_2/HfON/AlHfO/TaN [7]	8V 100µs/-8V 100µs	2.5	1.45	-	2.1@10^5

Table 1. Comparisons of P/E voltage, speed, initial ΔV_{th}, extrapolated for 10-year retention at 85 and 150°C and endurance.