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Monolithic integration of AlGaN/GaN HFET with MOS on silicon ⟨111⟩ substrates

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AlGaN/GaN HFETs and silicon MOSFETs have been integrated monolithically on a silicon ⟨111⟩ substrate. A differential heteroepitaxy technique was used to grow AlGaN/GaN HFET layers on silicon ⟨111⟩ substrates while leaving protected areas of atomically smooth silicon in which MOSFETs are built.

Introduction: AlGaN/GaN heterostructure field effect transistors (HFETs) have attracted much attention in recent years owing to their high breakdown voltage and high temperature operation capability compared to transistors in other material families. However, existing AlGaN/GaN HFET technologies tend to be poorly suited to integration of digital or mixed-signal circuits, limiting the applications of these devices. This Letter reports the first monolithic integration of AlGaN/GaN HFETs with silicon MOSFETs using differential heteroepitaxy on ⟨111⟩ silicon substrates [1]. Integrating both technologies allows for an expanded set of applications that can take advantage of the high voltage and high power handling capability of AlGaN/GaN HFETs as well as the high density, simplicity and low power consumption of MOS digital circuitry. An example of such an application would be to integrate CMOS DSP circuitry with a GaN-based power amplifier for transmit modules in wireless telecom systems. This would extend the work of Matsunaga *et al.* who used a hybrid chip which combines a class-B GaN PA with a CMOS circuit to provide dynamic biasing in order to improve linearity and efficiency [2]. Additionally there is great interest in GaN-based chemical, gas, biological, pressure and mass sensors [3, 4]. This work opens the door for the integration of MOS devices along with a GaN-based sensor, allowing for compact, low power read-out circuitry. An alternative hybrid approach to AlGaN/GaN HFET integration with CMOS was reported recently by Chung *et al.* [5].

Device fabrication: Decomposition of the GaN material system during the high thermal budget required in MOS processing, particularly during thermal oxidations (field and gate oxide) and implant annealing, is the primary obstacle to be overcome in accomplishing monolithic HFET/MOS integration. Fortunately CMOS thermal budgets have been reduced drastically in recent years through the adoption of techniques such as implanted retrograde wells, shallow trench isolation (STI) and even gate dielectric deposition. Integration here was based on relatively old MOS technology with 25 nm thermal gate oxide. Since STI was not available, enclosed geometry MOSFETs were used to avoid the thermal budget required for thick field oxide growth.

AlGaN/GaN layers were grown by ammonia-MBE on 50 mm diameter 10kΩcm silicon ⟨111⟩ substrates using the windowed growth technique described in detail in [6]. It should be possible to scale the growth technique to the much larger silicon wafer diameters used in commercial CMOS [7]. The GaN stack consists of alternating AlN and GaN stress relief layers followed by a 1.4 μm C-doped semi-insulating GaN buffer, a 200 nm undoped GaN channel layer and a 20 nm $Al_{0.3}Ga_{0.7}N$ cap. Areas in which MOSFETs were to be formed were protected by a 1.8 μm PECVD silicon dioxide layer overlaid with 100 nm sputtered *a*-Si during AlGaN/GaN layer growth. MOSFET areas were then selectively exposed by wet chemical etching of the PECVD silicon dioxide, lifting off the *a*-Si and overgrown GaN layers. To obtain useful MOSFET threshold voltages and avoid short channel effects silicon doping in the near-surface region was increased by a series of $^{11}B^{+}$ ion implants to form a retrograde well. The 25 nm thermal gate oxide was then grown at 900°C in dry oxygen, followed by a 900°C nitrogen anneal to reduce oxide fixed charge. Undoped polysilicon was then deposited by LPCVD at 625°C and etched in CF_4/O_2 plasma to define gate electrodes. Source/drain regions were formed by diffusion from a $POCl_3$ source for 30 min at 900°C giving a sheet resistance of 33 Ω/square. A borophosphosilicate glass (BPSG) layer was then deposited to protect the MOSFETs during HFET processing and flowed to smooth surface topography. The total thermal budget for MOSFET formation including BPSG flow was 900°C for 90 min.

HFETs were formed following the process described in [8]. These devices were mesa isolated with chemically assisted ion beam etching (CAIBE). An evaporated Ti/Al/Ti/Ag stack [9] with HCl pre-treatment was used to form source/drain ohmic contacts. A Pt-based Schottky gate metal was evaporated. It should be noted that gold is not used in the metallisation scheme to avoid minority carrier lifetime degradation and junction leakage in the silicon devices. A cross-section through the completed device structures is shown in Fig. 1.

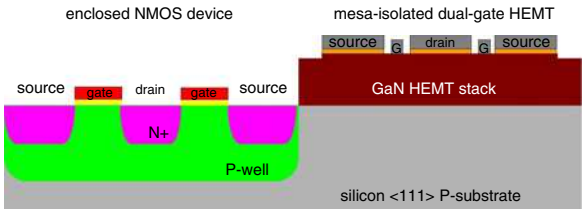

Fig. 1 *Cross-section of integrated devices*
NMOS device shown on left, mesa-isolated GaN HEMT on right

Results: Fig. 2 shows the drain characteristic of a typical HFET with gate length of 0.8 μm and width of 40 μm. The saturation drain current is 0.45 A/mm for $V_G = 0$, with a pinch-off voltage of −5 V. Further optimisation of the Ag-based ohmic contact is required and would be expected to result in improved drain currents

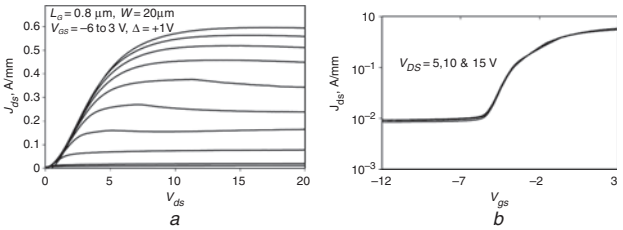

Fig. 2 *DC I-V characteristic and pinchoff of GaN HEMT device*
a DC I-V characterictic
b Pinchoff
$L_G = 0.8$ μm, $W_G = 80$ μm

Fig. 3 shows the drain and subthreshold characteristics of a typical MOSFET with length of 12.5 μm and width of 280 μm. The threshold voltage is approximately 0.3 V, which is consistent with TSuprem simulation. The maximum channel effective electron mobility estimated from the peak transconductance is 498 $cm^2V^{-1}\,s^{-1}$, indicating that the oxidation process has produced relatively low interface trap densities D_{it} and that the silicon surface in the window has not been damaged during the AlGaN/GaN layer growth. A subthreshold swing (Fig. 3*b*) of 80 mV/decade is also measured, confirming low D_{it}.

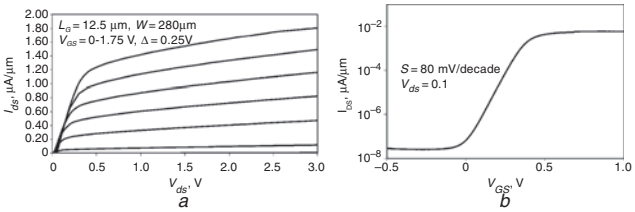

Fig. 3 *DC I-V characterictic and subthreshold of enclosed NMOS device*
a DC I-V characterictic
b Subthreshold
$L_G = 12.5$ μm, $W_G = 280$ μm

The use of a ⟨111⟩ substrate is, of course, expected to give higher D_{it} than would the ⟨100⟩ substrates employed for most CMOS technologies. The use of ⟨110⟩ silicon substrates to take advantage of higher carrier saturation velocities than provided by ⟨100⟩ material is now being considered for state-of-the-art CMOS technologies. AlGaN/GaN heteroepitaxy has been demonstrated on ⟨110⟩ silicon substrates [10], so it is plausible that AlGaN/GaN HFETs could eventually be integrated with advanced CMOS without a significant penalty in MOSFET performance.

Conclusion: The first monolithic integration of AlGaN/GaN HFETs and silicon MOSFETs using heteroepitaxy on a silicon substrate is

reported. Protection of the MOSFET regions with a thick PECVD oxide overlaid with *a*-Si during growth of the AlGaN/GaN layers combined with thermal budget minimisation during MOS processing are the keys to accomplishing this integration. HFET performance was not compromised by the integration. High channel electron mobilities were obtained in the MOSFETs, evidence of the quality of the silicon surface preserved in this process.

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One or more of the Figures in this Letter are available in colour online.

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