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On the existence of submicron diameter current shunts in morphologically perfect device layers

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ABSTRACT

We investigated the origin of so-called “hot-spots” in large area pixelless QWIP-LED upconverter devices, which are quantum well infrared photodetectors grown in series with a light emitting diode [E. Dupont et al., *IEEE Photonics Technol. Lett.* 14 (2002) 182]. The hot-spots, with surface densities varying from 20 to 3000 cm^{−2} for the wafers studied, are LED electroluminescence singularities, which can be readily observed at temperatures below ~100 K. Their spatial FWHM is less than 1 μm and they can have peak intensities of more than three orders of magnitude higher than the uniform background emission caused by the dark current through the QWIP device. In most cases the hot-spots were observed on mirror smooth, morphological defect-free surfaces. These electroluminescence abnormalities result from highly localized electron injection channels in the QWIP portion of the device. As there is no morphological abnormality in their locations, these defects are undetectable with established wafer screening instruments such as Nomarski and Surfscan, yet may be very common in MBE-grown heterostructures. Although correlation with dislocations is observed, the great majority of dislocations do not give rise to the hot-spots, and there are many hot-spots, which are not located in the proximity of any dislocation. We therefore, propose that the hot-spots arise from a local alloy separation in ternary layers, induced by floating organic molecules or molecular contamination clusters, resulting in nanowire-like defects. Highly localized drops in the layer resistivity caused by such defects will adversely affect the performance of any devices relying on vertical transport, particularly if the device current depends very strongly on the height of the potential barriers employed, such as in quantum well infrared photodetectors or resonant tunneling diodes. Also, for devices working at high current densities, such as certain lasers or HBTs, the presence of such defects may lead to early device failure.

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1. Introduction

Of all the epitaxial techniques, molecular beam epitaxy (MBE) arguably offers the greatest control for creating multilayer structures with arbitrary compositional profiles along the growth direction, while maintaining excellent lateral uniformity. This is particularly true for the AlGaAs/GaAs material system, where strain effects are small and uniform alloys can be obtained across the entire compositional range. It has long been recognized that point defects can have a detrimental effect on performance of devices relying on vertical electronic transport. Advancements in MBE technology and clean-room practices eradicated almost entirely such imperfections, and device layers with featureless, nearly atomically smooth surfaces, having total point defect

densities below 10 defects per cm² can be grown routinely. Yet obtaining devices over large wafer areas showing very uniform parameters and very high reliability is often difficult. These issues have frequently been attributed to problems related to device processing. However, recently statistical evidence was presented attributing the so-called infant mortality of InGaP/GaAs Heterojunction Bipolar Transistors (HBTs) to the detrimental effects of dislocations, which are present in GaAs substrates and propagate through the epitaxial layer [1]. In this work we present results pointing to another, so far not considered type of defect in epitaxial heterostructures, which can severely degrade the performance of devices relying on vertical transport.

In the recent past we have been developing large area (up to 1 × 1 cm²) pixelless mid-IR to near-IR upconverters [2,3]. These devices, which circumvent the hybridization with Si read-out circuitry necessary for standard pixilated Quantum Well Infrared Photodetector (QWIP) focal plane arrays, explore a different approach—reading the photocurrent map optically using an inexpensive high resolution CCD element. In the absence of an

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IR signal such a device should emit a uniform glow across its area. However, in practice we always see numerous “hot-spots” (Fig. 1a), which have to be “micromachined” out for the final device to function properly. Although the density of the hot spots and their intensities vary from wafer to wafer, we have seen them in all QWIP-LED wafers processed so far, regardless of whether they were grown in our MBE lab or purchased from MBE wafer foundries. All other characterization tools used on the

unprocessed layers, such as X-ray, SIMS, SEM, TEM, AFM, Nomarski, and Surfscan indicate excellent structural quality and mirror smooth featureless morphology with total point defect counts ranging from 2 to 30 cm^{-2} . Most of the wafers on which the present study is based have been used primarily for gaining understanding and optimizing other device characteristics. However, the large range of different parameters and procedures employed over the course of several years was aimed specifically at eliminating the observed hot-spots. The emphasis of the present work is on elucidating the nature and origin of these defects. Although no satisfactory remedy has been found yet, the results presented below can be of great importance to the semiconductor industry and point towards possible paths for elimination of these so far “invisible”, yet potentially detrimental, defects in heterostructures.

2. MBE growth and characterization

Most of the structures discussed in this section, unless otherwise stated, have been grown on a V90+ Oxford Instrument MBE system using 3" GaAs epi-ready substrates from three different vendors. All these substrates have been cut from boules grown using VGF (vertical gradient freeze) technology. Nominal etch-pit density (EPD) counts were less than 5000 cm^{-2} for semi-insulating (SI) substrates and less than 500 cm^{-2} for N+ substrates. We have performed growth on substrates with surfaces either nominally (001) or (001) off-cut 2° towards the $\langle 011 \rangle$ crystallographic direction. Some structures, which were purchased from MBE wafer foundries, were grown on LEC (Liquid Encapsulated Czochralski) SI substrates with a much higher nominal EPD of $50,000\text{ cm}^{-2}$. Substrates for structures grown in our laboratory were loaded into indium free molybdenum holders and transferred into the MBE system straight from the original packaging, in a clean-room environment. After initial outgassing at 150°C at the fast entry-lock, substrates were transferred into the preparation chamber's outgassing stage, where they were outgassed for 1 h at 400°C (thermocouple temperature) prior to being transferred into the growth chamber. Native oxide was desorbed using either standard thermal oxide desorption by a temperature ramp to 630°C under arsenic overpressure, or by pulsed Ga pre-deposition at 520°C , and subsequent annealing at 630°C under arsenic overpressure [4]. Growth temperature was monitored using the band-edge thermometry technique [5], and an IS4000 reflectance-compensated pyrometry system from SVT Associates. For all of the structures discussed, the Ga flux was kept constant throughout the growth, yielding a GaAs growth rate of 0.2 nm/s at 600°C , while the fluxes for other elements were adjusted appropriately for the desired layer composition or doping. Arsenic overpressure was one of the parameters we varied, and this was adjusted in the range from 1.5 to $6 P_0$, where P_0 is the minimum As overpressure needed to ensure group V stabilized surface reconstruction at 600°C during deposition of GaAs at 0.2 nm/s growth rate, as described in [6]. Veeco Mark IV or Mark V valved As cracker cells were used as the source of arsenic flux. Most structures were grown using an As_2 flux; however, some were grown using As_4 molecules. A Veeco dual filament SUMO source or an e-Science Titan dual filament source was used as a source of Ga, while Al was supplied using a 30 cc cold lip conical cell from Veeco, or an 85 cc dual filament conical cell from e-Science.

The typical QWIP-LED structure is shown in Fig. 2. Asymmetric Si-Delta doping has been employed to compensate for the Si segregation effect [7]. The growth temperature for the LED portion of the device was 600° , while the growth temperature for the buffer layer and QWIP sections was used as varying

Fig. 1. (a) CCD image of electroluminescence (EL) across $1.3 \times 1.3\text{ mm}^2$ window of $1.5 \times 1.5\text{ mm}^2$ device mesa. Under the biasing conditions and very low intensity diffused IR background, uniform EL is expected across the entire device. Note the numerous bright EL spots, majority of which are not related to any morphological surface feature. The dark spot on the image is attributed to a speck of dust on this particular device. A short integration time was used in order not to saturate the CCD signal at the hot spots locations. (b) The same EL map, as shown on pane a), represented as a surface plot of CCD counts. (c) Same as (b), but showing the full dynamic range. In this case the largest EL singularity has peak intensity 30 times that of the background. High resolution EL study shows the spatial FWHM of the EL hot-spots to be instrumentally limited (about $1\text{ }\mu\text{m}^2$), thus the actual brightness of the hot-spots at the peak is larger by at least two orders of magnitude.

parameter. Typically, the standard GaAs buffer layer was grown at 600 °C; however, we have also tried the effectiveness of low-temperature GaAs (LTG) buffer layers, and high temperature (690 °C) GaAs or GaAs/AlAs superlattice. The etch-stop, which was used for some QWIP-LED large area devices [3], was grown at 690 °C to ensure high quality AlGaAs in this difficult compositional range. The QWIP sections were grown at 550, 600 or 630 °C.

The routine post-growth wafer characterization involved: (i) conducting surface morphology inspection of the as-grown structures using Nomarski phase-contrast microscope equipped with 12-bit high-resolution CMOS camera, (ii) collecting maps of point defects over the entire 3" wafer using KLA Tencor Surfscan 6200, and (iii) taking X-ray diffraction rocking curves with Philips EM430T MRD instrument. SIMS, AFM and TEM analysis were performed on selected wafers. Cleaved wafers were subsequently processed into devices using standard microfabrication techniques [3]. As a qualification step before fabricating the large area devices, a test cluster of smaller devices was processed from each wafer (see Fig. 3a) and used for inspecting local structure

properties, such as I - V or electroluminescence (EL) uniformity. All of the images presented in the present work have been obtained from individual devices of such test clusters. Fig. 3b shows a Nomarski phase-contrast image of a $600 \times 600 \mu\text{m}$ device mesa. All devices shared a common bottom contact, while the top rectangular Ti–Pt–Au “frame” contacts visible in the image were individually wire-bonded to the pins on the chip mount.

For the study of hot-spot defects discussed here, reference Nomarski images of individual devices, such as that in Fig. 3b, were acquired right after processing. The device clusters were subsequently mounted on the cold finger of a liquid nitrogen cryostat facing the optical window. The strongest hot-spots start appearing below 100 K and, as the temperature is decreased, numerous and weaker hot spots show up due to an increase of the contrast between the hot spots and background emission of the healthy area of the device. The reported EL maps of the biased devices were obtained with a cold finger temperature of ~ 64 K (close to the triple point of nitrogen) using a 105 mm focal length Micro-Nikkor objective lens, and high-dynamic-range CCD camera (Andor iKon DW432 system equipped with a back-illuminated and AR coated 1125×1152 Marconi 55-30 chip with $22.5 \mu\text{m}$ large pixels saturating at 300 ke^- and cooled at -45°C). Subsequently, the device clusters were removed from the mount and subjected to a molten KOH treatment [8] to reveal locations of dislocation outcrops. With that approach three different maps of selected devices were collected, which could be directly overlaid on top of each other in order to inspect correlations between the hot-spot locations and positions of morphological defects or dislocations.

3. Experimental results

Fig. 1a shows an example of an EL map obtained on a $1.5 \times 1.5 \text{ mm}^2$ device mesa ($1.3 \times 1.3 \text{ mm}^2$ optical window). Apart from desired uniform background emission (expected from the uniform flow of dark current through the device) a constellation of very bright spots can be seen. Fig. 1b shows a surface plot of the CCD counts, while Fig. 1c shows a surface plot for the same device, but using full dynamic range of the observed features. At this

	layer	[nm]	Comments
LED	p-GaAs	15.0	Be-doped: $2 \times 10^{19} \text{ cm}^{-3}$
	p-AlGaAs	250.0	graded x: 0.24? 0.14, Be-doped: $1 \times 10^{19} \text{ cm}^{-3}$
	p-AlGaAs	100.0	x=0.24, Be-doped: graded 3×10^{18} ? $1 \times 10^{19} \text{ cm}^{-3}$
	AlGaAs	40.0	graded x: 0.10? 0.24
	GaAs	30.0	
	AlGaAs	40.0	graded x: 0.24? 0.10
QWIP 30 to 50 repeats	AlGaAs	35.0	x=0.24
	GaAs	4.4	
	Si-Delta		$3.0 \times 10^{11} \text{ cm}^{-2}$
	GaAs	1.0	
	AlGaAs	35.0	x=0.24
	n-AlGaAs	700.0	x=0.14, Si-doped $1.5 \times 10^{18} \text{ cm}^{-3}$
Optional Etch Stop, 250.0nm of AlGaAs x=0.45			
Buffer layer			
GaAs Substrate			

Fig. 2. Schematic of typical QWIP-LED structure used in this study.

Fig. 3. (a) Typical matrix of test devices used for this study. The largest device mesa was $1.5 \times 1.5 \text{ mm}^2$ in size. (b) Nomarski image for $0.6 \times 0.6 \text{ mm}$ device mesa. Note excellent surface morphology. Nomarski contrast was optimized for imaging morphological point defects.

magnification the spatial resolution of the map is limited by the image resolution (and effective pixel size of about $10 \times 10 \mu\text{m}^2$). Even under such imaging conditions the peak intensity of the brightest spot is 30 times that of the flat background. Inspection of the hot-spots under higher magnifications reveals that their spatial FWHM is in fact diffraction limited (about $1 \mu\text{m}$), thus for the case of the EL map shown, the actual peak intensities of the hot spots are at least two orders of magnitude larger. For this particular device cluster, the point defect density was less than 30 cm^{-2} , while the average density of hot spots was very high, about 3000 cm^{-2} , which is at the upper range of what we have observed. Coincidentally, this number is close to the area density of dislocations for the substrate used ($\text{EPD} < 5000 \text{ cm}^{-2}$ nominal). Typically, hot spot densities for wafers grown in our laboratory are between 50 and 1000 cm^{-2} , and no obvious correlation is observed with the expected dislocation densities in the substrate. While typical hot-spot densities measured on wafers obtained from epi foundries were also higher than 50 cm^{-2} , the smallest hot-spot count of 20 cm^{-2} was measured on one of the wafers purchased from IQE in 2000, which was grown on a substrate with an EPD of about $50,000 \text{ cm}^{-2}$.

Since the devices combine a QWIP and an LED, a natural question comes to mind: abnormality of which element in the structure is responsible for these hot-spots? It is obvious that the photons are emitted in the quantum well of LED, as this is the only location in the device where electrons and holes can recombine emitting photons at this wavelength. Albeit highly unlikely, the presence of ultra-clean clusters of material in the LED region cannot be entirely ruled out. To elucidate this question we have grown back-to-back a QWIP-LED device and an LED-only device, on two consecutive substrates from the same batch. The morphologies of both wafers examined by Nomarski and Surfscan were excellent, with mirror smooth surfaces and point defect counts of less than 8 per cm^{-2} . Subsequently, the wafers were subjected to the same processing protocol, and then biased with the same current density for the EL mapping at low temperature. The QWIP-LED devices showed numerous hot-spots ($\sim 700 \text{ cm}^{-2}$), while not a single hot-spot was detected on LED-only devices. This shows unambiguously that the LED hot-spots are basically manifestations of electron injection current singularities formed in the QWIP region. We measured L-I characteristics on our LED-only devices and found that over the four orders of bias current used, from 10^{-6} to 10^{-2} A/cm^2 , the CCD counts scaled perfectly linearly with the bias current. Thus, the surface plot of CCD counts shown in Fig. 1c is also an accurate representation of the injection current map for this device. Since the current density in the mesa was about $1 \times 10^{-3} \text{ A/cm}^2$, the peak current density at the brightest hot spot location was at least 3 A/cm^2 .

As we stressed earlier, the devices used in the present study typically were either completely free of any morphological abnormalities, or the observed point defect densities were much lower than the hot-spot densities. Thus, the great majority of hot spots are not related to any detectable morphological abnormalities. The only other defects, known to be present in epitaxial layers, with topology, which might be conducive to formation of such highly localized current injection threads are dislocations. Although it is well known that dislocations in semiconductors act as effective nonradiative recombination centres and minority carriers traps, there are no reports on possible current conduction along such crystallographic imperfections, giving us a unique opportunity to investigate this issue for the first time.

We, therefore, subjected devices with already mapped hot-spots to the dislocation-revealing molten KOH treatment. A high magnification Nomarski image of a representative resulting surface is shown in Fig. 4. Although the etched surface is no longer mirror-smooth, signatures of dislocation outcrops, in the

Fig. 4. Typical etch pits formed on our devices in molten KOH. The inverse pyramids with smooth facets, indicated on the image with arrows, are typical signature of dislocation outcrops and can easily be identified under Nomarski microscope.

Fig. 5. Overlays of EL maps with dislocation as revealed with KOH etch. The dislocation outcrops are marked here with black dots. Both images were obtained on the same structure on two different mesas. For this wafer the morphology of as-grown wafer was mirror smooth with overall average count of all defects (surfscan maps) below 8 per cm^{-2} , with 90% of all defects located at the edge of 3" wafer. No morphological defects have been detected on these mesas prior the KOH etch. (a) Small section of $1 \times 1 \text{ mm}^2$ device mesa with dense dislocation cluster. Here all hot spots are located on dislocations. Note that the number of dislocations is much greater than the number of hot-spots. (b) $600 \times 600 \mu\text{m}^2$ device. Note that here position of two hot-spots are coinciding with the positions of dislocations. However, the other two hot-spots are away from dislocation location. On this device 8 dislocations are detected, while only 4 hot-spots can be seen.

form of etch pits (here, inverted square pyramids with smooth facets), are clearly seen in the image. TEM studies performed on similar layers indicate that the structural defects responsible are in fact mixed type 60° dislocations with a screw component [9]. Fig. 5 shows overlays of the maps of the dislocation locations thus obtained with the maps of hot-spots for the same devices. Dislocation outcrops are marked in the figure with black dots. A strong correlation exists between the positions of the hot-spots and of the dislocations in the layer: for the map shown in panel (a) every hot-spot overlaps with a dislocation. However, note that the number of dislocations is more than twice the number of hot spots on this image. The correlation seen in panel (b) is weaker; only two of the four hot spots are located on a dislocation outcrop, while the remaining two are spaced far enough from the dislocations to safely exclude any direct association. There is no

Fig. 6. Two from the series of wafers studied here showed patches of α -type oval defects. This figure shows correlation of such oval defects with hot-spot location for $600 \times 600 \mu\text{m}$ mesa device. The oval defect positions are represented here with black ovals. (a) Note that all but one hot spots are associated with α -type oval defect, however, there are many more oval defects than hot-spots. The location of the hot spot on the perfectly smooth surface is indicated with an arrow. (b) Magnification of the small area showing the actual Nomarski image with the four α -type oval defect. Note that although morphologically the defects are identical, only two of them are coincident with hot-spots.

qualitative difference in this case between the hot-spots, which are co-located with dislocations (A) and those which are away from dislocations (B). Also, there is no qualitative difference between the KOH etch-pits for dislocations, which are associated with hot-spots (A) and those which are not (C). Although the exact proportions of A, B and C varies from wafer to wafer, or even from device to device, the qualitative observations are that while a correlation definitely exists, it is only partial.

Although most of the wafers grown for this study had excellent surface morphology, for a set of devices grown on one particular batch of SI GaAs substrates, patches of small α -type [10] oval defects were detected. In Fig. 6a we show an overlay of the defect locations and the hot-spots. Here we indicate the positions of the oval defects with black ellipses. Fig. 6b shows a magnified selection from the wafer, with the original Nomarski phase-contrast image of the area, where four α -type oval defects can be identified clearly. In the image (a), a correlation between the hot-spots and oval defects, much as for dislocations, is clearly visible but partial. There are many more oval defects than hot-spots, and there is one hot-spot in the image (shown with an arrow), which is not in the proximity of any oval defect. Also, as for dislocations, there is no qualitative difference between the hot spots located on the oval defects and those located away from one; nor there is any apparent morphological difference between oval defects associated with hot-spots and these which are not.

4. Discussion of the results and proposed model

Fig. 7 depicts our understanding of the type of heterostructure defects, which would give rise to the observed hot-spots. What effect could possibly lead to formation of such defects in heterostructures? A high-conductance channel along a dislocation seems to be a natural candidate, however, it is clear from the experimental results that for most of dislocations, the current density is not measurably larger than the background dark current. The very high contrast ratio between the normal dark current through QWIP and the current in hot-spot region, points towards an existence of a local “hole” in the barrier as the most plausible explanation. Indeed, for a QWIP the dark current is mainly caused by the thermal escape of carriers from the wells (i.e. above the barrier) and depends exponentially on the barrier

Fig. 7. (a) Expected uniform dark current through the QWIP, and related uniform Near-IR emission from LED. (b) The proposed mechanism behind the hot spot formation: low resistance paths are present in the QWIP stack, which allow much higher local current injection. This can take place if the effective heights of the AlGaAs barriers are lower along such paths.

height. At 64 K, a local change of barrier composition from $x=0.24$ to 0.22 would result in forty-fold increase of dark current through the device [11]. For another 2% drop in Al composition, this number would increase to sixteen hundred, which is enough to explain the typical brightness of the hot-spots we observe. From the spatial FWHM of hot-spots we conclude that such “holes” in our barriers must be smaller than $1 \mu\text{m}$ in diameter, and likely much smaller. For a sufficiently small size of such a barrier fault, quantum effects will start to play an increasingly important role. This will tend to moderate such a drastic increase in the local conductance with lowering composition. While different scenarios can be modelled to gain a deeper understanding of such processes, it is immediately clear that a local drop in composition of the barrier gives ample room for hot-spot formation. From the material science point of view, the important question is what possible mechanism could lead to formation of such a local composition drop. The character of the hot-spots and their very low density (as compared with the surface atom density) excludes random alloy fluctuations or any kind of phase separation from the list of likely culprits. A possibility is the presence on the surface of large Ga clusters ejected from effusion cell—should such a cluster land on the wafer at the start of the barrier growth, it would provide a local source of Ga, effectively lowering the barrier composition in its vicinity. However, this effect can be excluded because of the strong correlation of the hot spots with dislocations. One would expect such clusters to land on the surface randomly, and it would be impossible under arsenic-rich growth conditions for a Ga cluster to migrate tens of microns and anchor itself at the dislocation outcrop.

With dislocations and gallium clusters ruled out, there appears to be no other mechanism in the *known* epitaxial growth effects portfolio, to explain the existence of the observed hot-spots. Below we propose a defect formation process, which can consolidate all our experimental findings and to the best of our knowledge has not been considered yet.

It is well known that substrate surfaces, even freshly cleaned, are not free of contaminants. Indeed, it is very hard to control surface preparation to the degree, which would ensure an atomically clean surface covered with an atomically clean native oxide. Thus, optimization of the surface cleaning for epi-ready substrates stops when smooth morphology, point defect free layers can be grown on them reproducibly. SIMS profiles of epitaxial layers always show an accumulation of contaminants at the interface with the substrate; however, there are no reports on the spatial distribution of such contaminants. Oxygen, carbon and silicon are routinely seen at levels in excess of 0.1 monolayer and these are likely to be present in the form of organosilicon

compounds and organic molecules or molecular clusters. In-situ cleaning should be able to lower their levels, however, few MBE systems are equipped to perform such procedures. SIMS profiles indicate that most of that contamination is buried at the substrate–layer interface, and not much attention has been given to possible segregation of contaminants towards the growth surface. Another common epi-wafer contaminant has recently been identified, namely calcium, probably left on the surface from wafer polishing routine [12,13]. SIMS studies indicated that even though some calcium is buried at the substrate–layer interface, a large fraction floats on the growing layer surface, with no detectable tendency for incorporation into either GaAs or AlGaAs at typical growth temperatures. An incorporation of calcium from the floating layer was detected at growth temperatures lower than 450 °C, as well as during growth of dilute nitrides, and to some degree at GaAs/AlGaAs interfaces. As layer compositions, interfaces and growth conditions for our QWIP-LED structures are similar to those described by the authors reporting these effects [12,13], it is very likely that calcium related contamination floats on our layers also. However, this is unlikely to be responsible for the observed hot-spots, since the thick low-temperature GaAs buffer we employed for some of the structures should have trapped any calcium related contamination [13], but no apparent reduction in hot-spot density was detected. Nevertheless, the documented presence of such a floating contamination points to other possibilities which must be considered.

The highly competitive Si industry for decades now has been under pressure to reduce device sizes and improve their reliability, lowering their cost at the same time. Particulate contamination was recognized early on as the key element, which needs to be brought under control. However, in the 90's it became apparent that another, much harder to control contaminant had to be seriously addressed, namely volatile organic molecules [14]. Personnel in the cleanrooms is a significant source, however, outgassing from all kinds of plastic tools and containers can be the largest problem. Although many volatile organic molecules will tend to adhere to the wafer surface, long-chained molecules with heteroatoms and highly polar functional groups will stick particularly effectively, because of their much stronger van der Waals bonding. The strength of such bonding, along with good thermal molecule stability, is often sufficient for the contamination to survive all stages of wafer preparation, including thermal oxide desorption or even UV/ozone treatment [14].

We believe that a model involving such long-chained polar molecules floating on the growing surface can provide an adequate explanation of all our experimental results. An inert floating molecule will likely have little effect on the growth of GaAs epitaxial layers, but it can have a very strong influence on the growth of AlGaAs layers in its immediate vicinity; and the larger the molecule, the stronger effect it will have on the alloy. In the simplest case, such a molecule or molecular cluster will prevent the atomic flux supplied by the effusion cells from reaching the area under it. Thus, the atoms for the layer forming under the contaminant will have to come from the immediate vicinity on the surface. Since Ga atoms are much more mobile than Al, they will be predominantly used for the growth of the layer under the molecule. The resulting modification such a process would bring to the heterostructure is schematically illustrated in Fig. 8. A kind of wire is expected to form in the AlGaAs barriers of our QWIP region, with Al-enriched walls and an Al-depleted inner core. This is exactly what we need to explain formation of high current filaments in the QWIP region, and the resulting hot-spots in the LED region. Within such a model one can also explain the strong correlation of the hot-spots and the dislocations. The latter are expected to be charged [15], thus giving rise to a long-range Coulomb potential, which will tend to

Fig. 8. Schematic representation of one of the plausible processes which may lead to formation of vertical conductive paths in heterostructures. (a) “Normal” epitaxial process for the growth of GaAs/AlGaAs multiple quantum well stack. (b) Perturbation expected in the presence of thermally stable molecule floating on the growing surface. In this situation fewer Al atoms are going to be built-in under the molecule because of the combination of flux shielding and low surface mobility of Al atoms compared to Ga atoms. This lower composition inner core is expected to be surrounded by higher than average Al composition walls, preserving total number of Al atoms in the layer.

polarize the molecule floating on the surface in its vicinity, attracting it to the dislocation outcrop as the growth progresses, and eventually anchoring it there for the remainder of the growth. It is also possible that such a net localized charge at the dislocation will facilitate the sticking of polar molecules floating in the air or outgassed from substrate containers. A process such as this could provide an explanation of the correlation of the infant mortality of HBTs and dislocation density in the substrates, as reported by Alt et al. [1]. This would imply that resolution of this important problem would be improving the substrate cleaning, not the lowering of dislocation density in the substrate.

Note that in order to have such a localized strong current injection from the QWIP into the LED, the high-conductance region does not have to propagate through the entire stack. The doping in the wells ($3 \times 10^{11} \text{ cm}^{-2}$) is sufficient to provide independent reservoirs of electrons capable of feeding the hot-spot. This is important, since individual floating molecules can aggregate into larger clusters during the growth of the QWIP stack, giving rise to a wide range of conductive wire sizes and lengths, explaining the large variations observed in the hot-spot intensities.

The last experimental result we discussed, and at first sight, the most difficult to reconcile with the above model, is the partial correlation of the hot spots with α -oval defects, shown in Fig. 6. The explanation needed here is provided by the elegant paper by Takagishi et al. [9] addressing the origin of this exact type of morphological defect. As shown in this work, α -oval defects are in fact the products of the screw component of the mixed dislocations, and are probably related to the spiral growth such dislocations may induce on the epitaxial surface. Our observation that the correlation between the hot-spots and α -oval defects is similar to that seen for dislocations is consistent with Takagishi's one-to-one correspondence between dislocations and α -oval defects. Since for most depositions we do not observe such surface defects, it is clear that they do not always form on the surface in the presence of dislocations. It is likely that the presence of some other type of surface contamination can trigger such a morphological instability at dislocation sites [16] through alteration of surface kinetics. Surface kinetics can of course also be

altered by changing the growth conditions. For the two structures where we do observe α -oval defects, a much higher than typical As overpressure of $6P_0$ was used. Such an overpressure reduces the Ga atoms surface diffusion length [17], and will lead to tightening of the spiral growth around screw dislocations [18], increasing the likelihood of hillock formation, in support for Takagishi conclusions.

It is important to stress that the proposed model of hot spot formation has been arrived at through the elimination of known plausible mechanisms. Even though the invoked processes involving floating molecules are all possible in the light of other experimental data, we do not present results unambiguously proving that this is indeed the case. Clearly more work is needed to fully resolve this issue. The main difficulty lays in the relatively low concentration of these defects and the lack of morphological signatures to aid in their localization, necessary for microscopic studies. Even if the defect location was marked, say by laser ablation during low-temperature EL mapping, TEM contrast for such a small compositional anomaly in the presence of noise caused by the milling or focused ion beam damage, would be too small to register. With these challenges, the most promising for further studies appears to be pursuing the in-situ pre-cleaning methods followed by presented here QWIP-LED growth and inspection.

5. Conclusions

In this study we have observed a class of defects, previously undetected yet probably very common in MBE-grown heterostructures. Such defects are tentatively attributed to the local alloy separation in ternary (or quaternary) layers, induced by floating molecules or molecular contamination clusters. This proposed process would result in the formation of submicron diameter wires with cores made of material having a lower bandgap than intended. As shown experimentally, such nanowires are capable of shunting currents by several orders of magnitude higher than the neighbouring “perfect” material. Their nature can adversely affect the performance of devices relying on vertical transport, particularly if the device current depends very strongly on the height of potential barriers employed, such as in QWIPs or resonant tunneling diodes (RTDs). For many other heterostructure-based devices, such defects, because of their submicron diameter and low surface density, may have little or no effect on their parameters. However, for devices working at high

current densities, such as certain lasers or HBTs, the presence of nanowire defects may lead to early device failure.

Results presented for the cross-correlation between these defects and the dislocation outcrops revealed that dislocations normally do not conduct excess current under bias in our devices. The observed partial correlation between the nanowire defects and dislocation outcrops has been attributed, within the proposed model, to the tendency for dislocations to attract and anchor the floating contamination responsible for nanowire formation.

The presented results identify a unique tool for detecting nanowire defects, namely large area pixelless QWIP-LED structures. A much simplified version, with a single doped quantum well below the LED, may be equally effective, and could facilitate greatly further optimization of substrate preparation processes for the compound semiconductor industry.

Although the nanowire defects were studied here in the context of their parasitic influence on devices, the postulated mechanism for their formation, if correct, could be exploited in a deliberate way, opening up new paths for fabrication of quantum wires.

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